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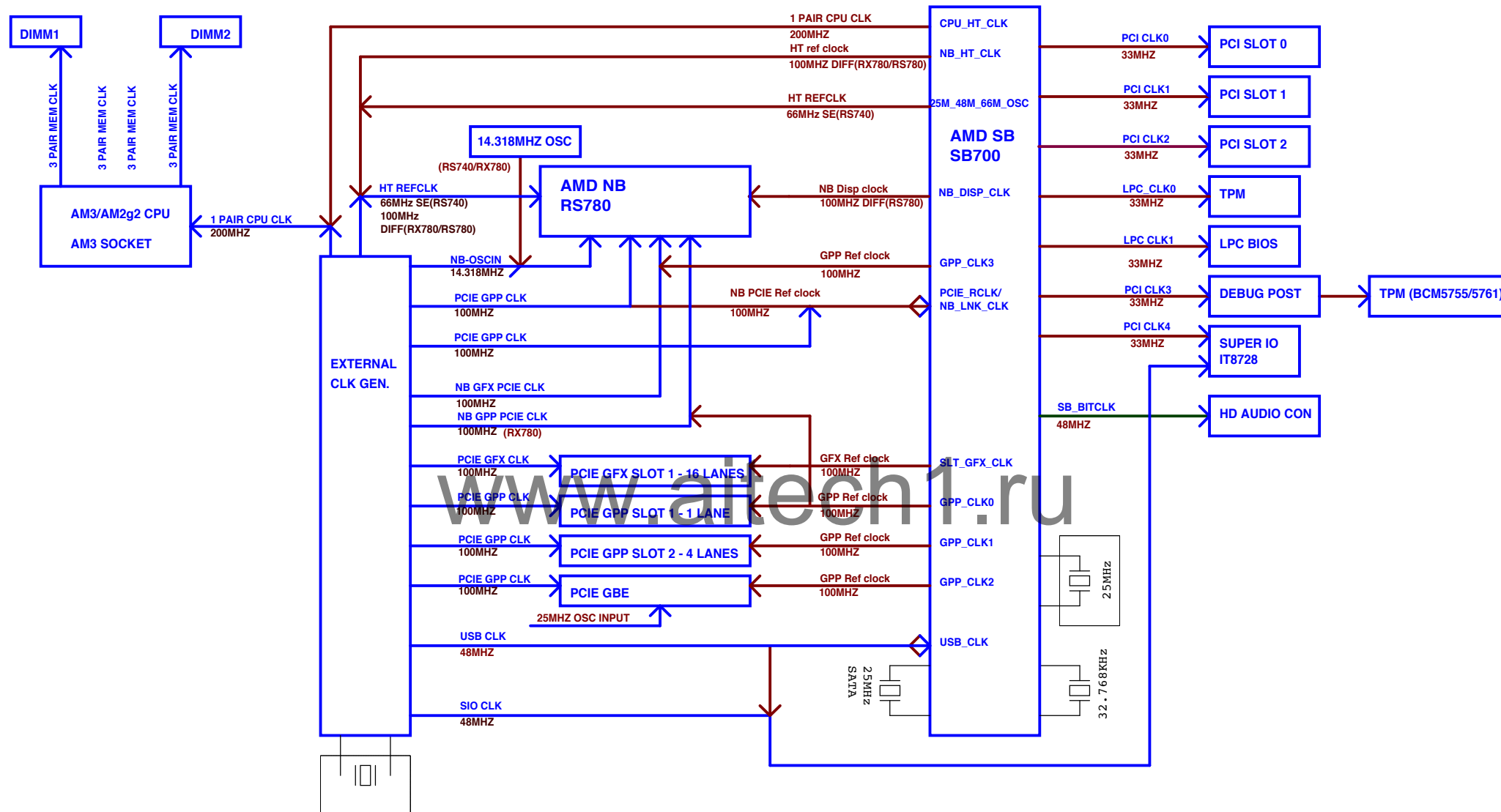
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C

B

A



External clock mode

Internal clock mode

Title CLOCK DISTRIBUTION			
Size	Document Number	Rev	
Custom	AA55C-A1S	6.0	
Date:	Friday, July 29, 2011	Sheet	4 of 45

V0.60:
Base on Standard circuit.

Ver0.61:
1.Gigabit LAN From APU_GPP3 to GPP2;
2.del STAT3,USB 3.0 SILKSCREEN.
3.add GR23/GR25 FOR matching DVI MONITOR.
4.change YR7 for detect APU_VDDNB_RUN.
5.change GR7/GR8 from 4.7k to 5.1k.
6.add YR50,YR152:0/NI for PME Function,
7.R3: From 1.1k to 1k 1% FOR +1.1V_ALW.
8.add EC20 FOR PCI_AD31.
9.REAR USB3.0 USE USB2.0 FUNCTION.
10.+1.1V_RUN use VIN4 instead of VIN6.
11.add SC21---->NI for Measuring T14.
12.JFRONT_USB3_1---->NI,parts circuit NI.
13.R79/R80/R81/Q121/Q122/C118
---->NI FOR PWRGD_PS control SB_PWRGD.
14.PWM compaesation R/C network change for ST6717A
15.MEMORY Voltage default from 1.55 to 1.6V.
change MR17/MR18,MR22/MR23/MR24.
16.change EUPR5 From 4.7k to 10k. for prevent drop.

ECN:

2011-07-26:
PEX16-2
From PCIEX16-164 PIN-B to PCIEX16-164 PIN-R.

2011-07-26 pm:
MOSFETHEATSINK
20-120-105300H1 MOSHS-AA75B
MOS 汎 /?伎 /105.3x30.7x22.3mm/(0288-0175F)/(HF)/.KG
-----> 20-120-981500H11 MOSHS-A88PC
MOS 汎 98.26x15.5x18mm/?伎/遷澄/ 糯 /H1-NB384-HS01/. 扭

www.vinafix.vn

www.aitech1.ru

Ver6.0:
1.REAR USB3.0 location:USB1.
2.SR12:PU from 3.3V_STBY to 3.3V_DUAL,
3.remove CIR Header.
4.ADD R82 PU to +3.3V_DUAL
5.ADD PCT13/PCT14 FOR APU_VDDNB_RUN.
6. LOCATION change:
DIMM_A0--->DIMM_A1,DIMM_A1--->DIMM_A2,
DIMM_B0--->DIMM_B1,DIMM_B1--->DIMM_B2,
7.all RN---->Single Resitor.

V6.0 EMI SOLUTION:

1.ADD SC22 :FOR CLK_48M_SIO
2.ADD SC28:close to SFB1.
3.ADD CC83/CC86:
4.ADD SC29: FOR -XRI1 SWAP LAYERS
5. ADD YC87/YC88/YC89:FCH_VGA_R/G/B

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REVISION HISTORY			
Size Custom	Document Number AA55C-A1S		Rev 6.0
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5

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CPU1H

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PEX16

27 GFX_RX0P
27 GFX_RX0N
27 GFX_RX1P
27 GFX_RX1N
27 GFX_RX2P
27 GFX_RX2N
27 GFX_RX3P
27 GFX_RX3N
27 GFX_RX4P
27 GFX_RX4N
27 GFX_RX5P
27 GFX_RX5N
27 GFX_RX6P
27 GFX_RX6N
27 GFX_RX7P
27 GFX_RX7N
27 GFX_RX8P
27 GFX_RX8N
27 GFX_RX9P
27 GFX_RX9N
27 GFX_RX10P
27 GFX_RX10N
27 GFX_RX11P
27 GFX_RX11N
27 GFX_RX12P
27 GFX_RX12N
27 GFX_RX13P
27 GFX_RX13N
27 GFX_RX14P
27 GFX_RX14N
27 GFX_RX15P
27 GFX_RX15N

GFX_RX0P
GFX_RX0N
GFX_RX1P
GFX_RX1N
GFX_RX2P
GFX_RX2N
GFX_RX3P
GFX_RX3N
GFX_RX4P
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GFX_RX13N
GFX_RX14P
GFX_RX14N
GFX_RX15P
GFX_RX15N

AF8 P GFX_RXP0
AF9 P GFX_RXN0
AE7 P GFX_RXP1
AE8 P GFX_RXN1
AD5 P GFX_RXP2
AD6 P GFX_RXN2
AD8 P GFX_RXP3
AD9 P GFX_RXN3
AC7 P GFX_RXP4
AC8 P GFX_RXN4
AB5 P GFX_RXP5
AB6 P GFX_RXN5
AB8 P GFX_RXP6
AB9 P GFX_RXN6
AA7 P GFX_RXP7
AA8 P GFX_RXN7
Y5 P GFX_RXP8
Y6 P GFX_RXN8
Y8 P GFX_RXP9
Y9 P GFX_RXN9
W7 P GFX_RXP10
W8 P GFX_RXN10
V5 P GFX_RXP11
V6 P GFX_RXN11
V8 P GFX_RXP12
V9 P GFX_RXN12
U7 P GFX_RXP13
U8 P GFX_RXN13
T5 P GFX_RXP14
T6 P GFX_RXN14
T8 P GFX_RXP15
T9 P GFX_RXN15

Modify:2011-06-01,V0.61.

GPP_APU_RX0/TX0:PEX1.1.

GPP_APU_RX1/TX1:PEX1.2.

GPP_APU_GBE_RX2/TX2:Gigabit LAN44

29 GPP_APU_RX0P
29 GPP_APU_RX0N
29 GPP_APU_RX1P
29 GPP_APU_RX1N
29 GPP_APU_RX2P
29 GPP_APU_RX2N
29 GPP_APU_RX3P
29 GPP_APU_RX3N

GPP_APU_RX0P
GPP_APU_RX0N
GPP_APU_RX1P
GPP_APU_RX1N
GPP_APU_RX2P
GPP_APU_RX2N
GPP_APU_RX3P
GPP_APU_RX3N

AH5 P GPP_RXP0
AH6 P GPP_RXN0
AH8 P GPP_RXP1
AH9 P GPP_RXN1
AC7 P GPP_RXP2
AC8 P GPP_RXN2
AF5 P GPP_RXP3
AF6 P GPP_RXN3

APU_VDDP_B_RUN CR1

APU_PCIE_P_ZVDD

196 1% 0402

Place Within 1.5" from APU

196 OHM for DG required

APU>

SOCKET FM1 905 SMD

P_VDDDP

P_ZVSS

P_VSS

P_VSS

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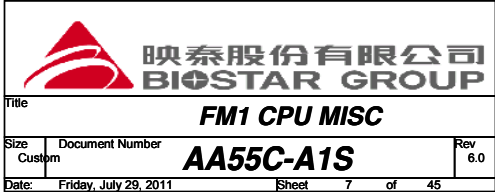
P_VSS

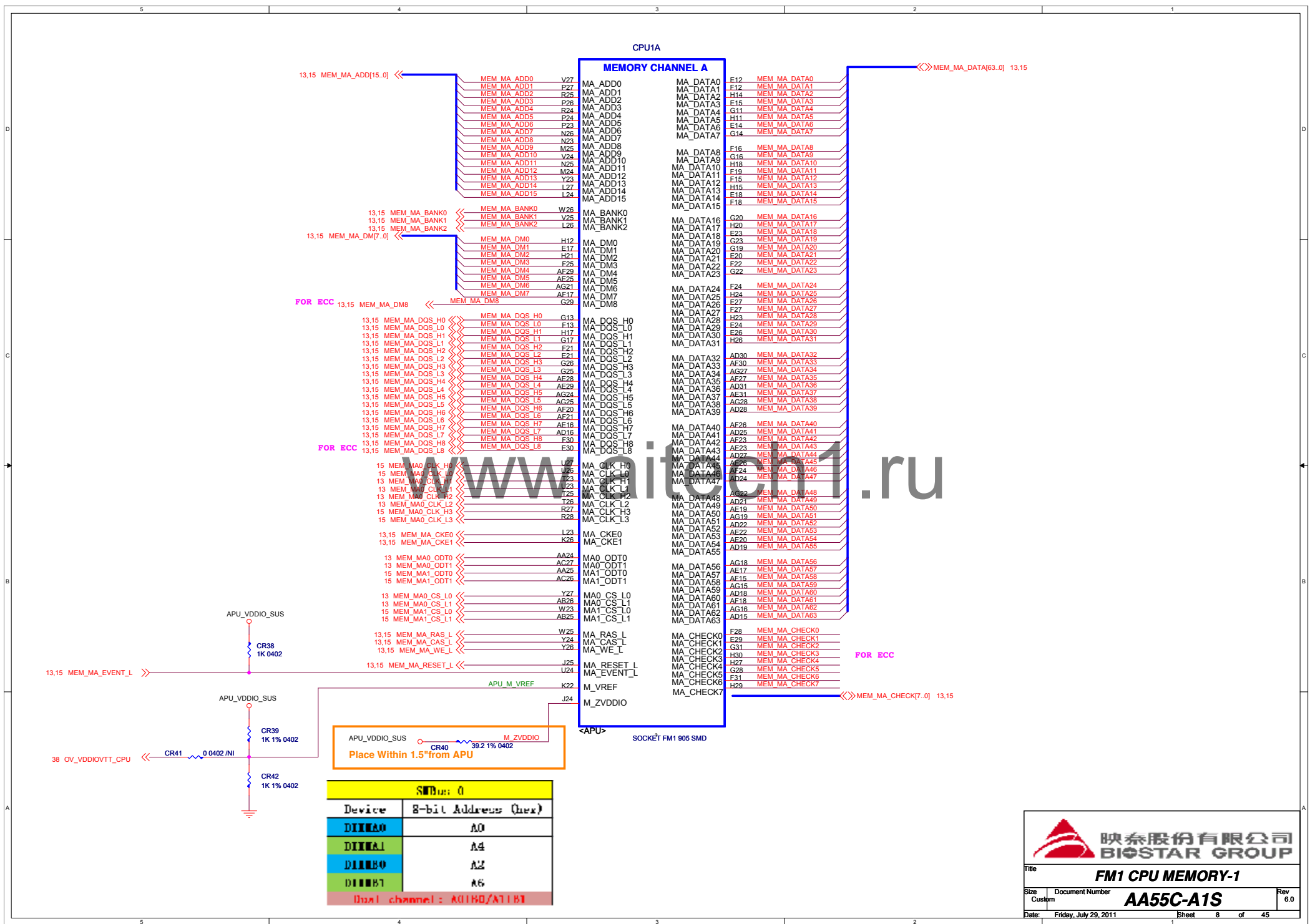
P_VSS

P_VSS

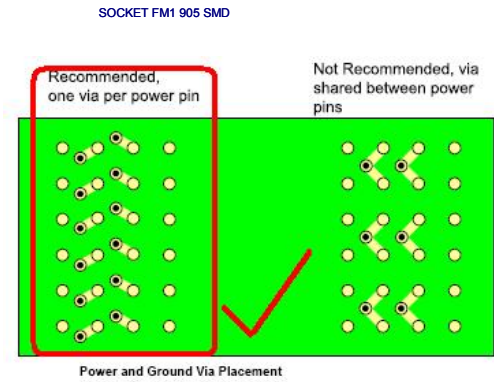
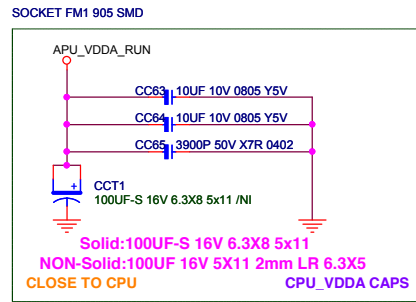
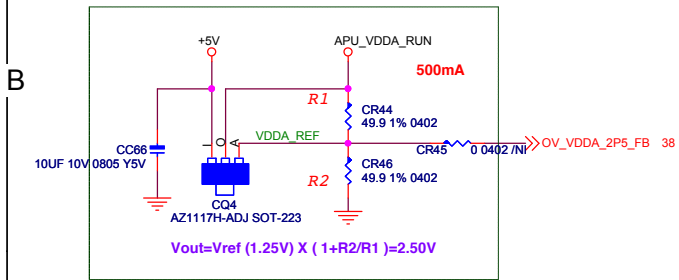
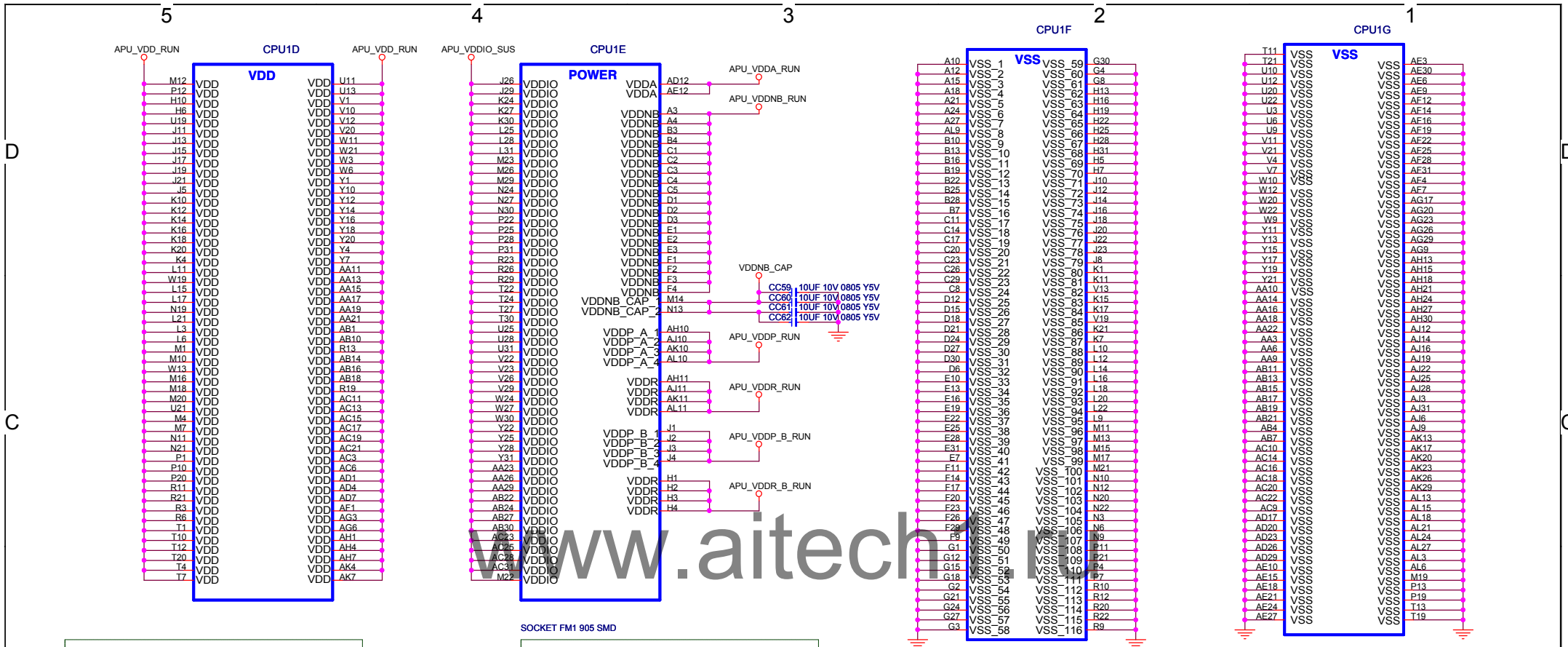
P_VSS

P_VSS









	FM1									
	VSS	VDD	VDDNB	VDDIO	VDDP	VDDR to VSS		VDDA	Mvref	
Total Power Pins	416	226	102	19	51	8	8	4	4	2
Value/Size/Material										
22uF/1206/X5R		11	2	4	-	1	-	-	-	-
10uF/0805/X5R		2	1	2 + 1(B)	1	-	-	-	-	-
4.7uF/0805/X5R		3	1	4	2	2 + 2	2	2	1	-
0.22uF/0603/X5R		2	2	2 + 2	2	2 + 2	2	2	1	-
0.1uF/0603/X5R		-	-	-	-	-	-	-	-	1
0.01uF/0603/X5R		4	-	-	-	-	-	-	-	-
3.3nF/0603/X5R		-	-	-	-	-	-	-	1	-
1nF/0603/X5R		-	-	-	4	-	-	-	-	1
180pF/0402/C0G		3	1	2 + -	4	2	-	-	-	-

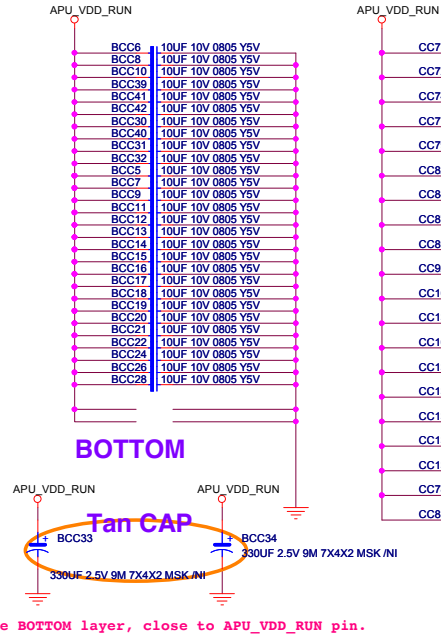
映泰股份有限公司
BIOSTAR GROUP

Title: **K8 CPU POWER**

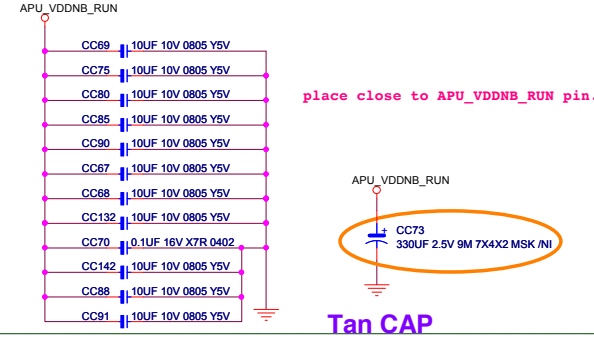
Size: Custom Document Number: **AA55C-A1S** Rev: 6.0

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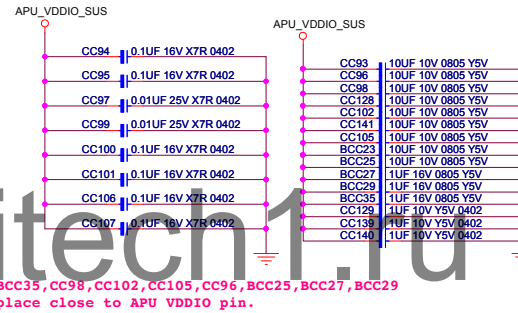
APU_VDD_RUN (CPU CORE)



APU_VDDNB_RUN

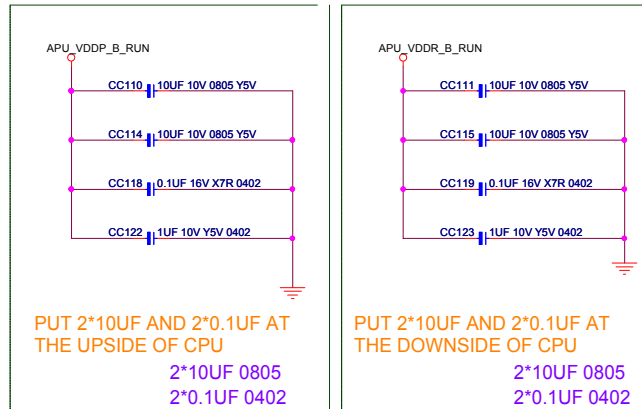
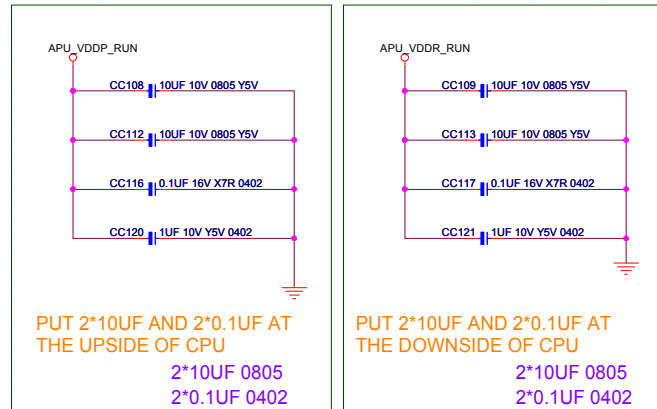


APU_VDDIO_SUS



APU_VDDP_RUN, APU_VDDR_RUN


place TOP layer, close to APU_VDDP_RUN pin.



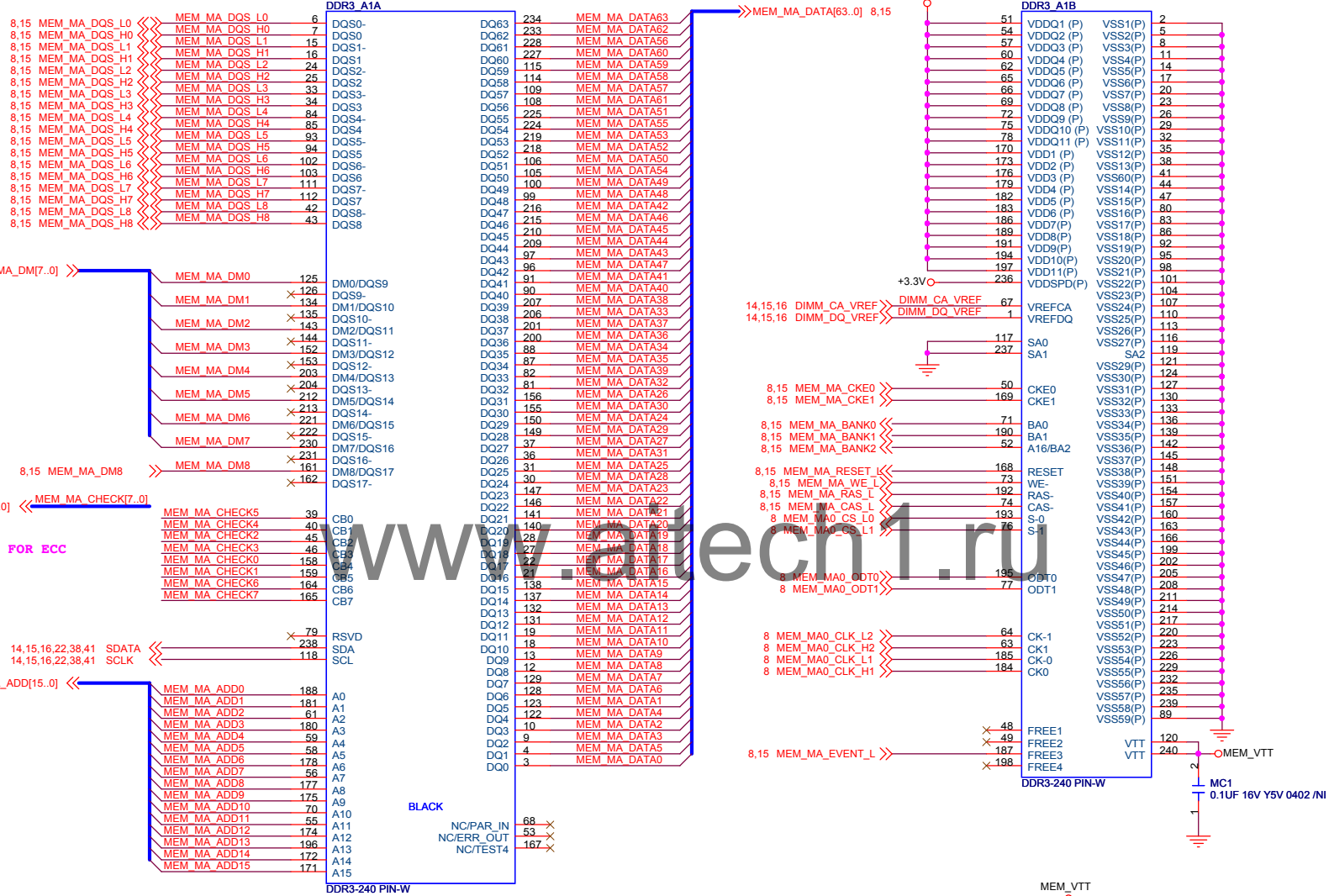
BIOSTAR STANDARD
NO:2011_AMD_FM1_01


APU DECOUPLING CAP		
File	Document Number	Rev
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Title DDR CAP BYPASS		
Size Custom	Document Number AA55C-A1S	Rev 6.0
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DDR3_A1





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BIOSAR GROUP

Title		
DDR DIMM-1		
Size	Document Number	Rev
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DDR3_B1

DDR3_B1A

9,16 MEM_MB_DQS_L0 <<> MEM_MB_DQS_L0 6 DQS0-
9,16 MEM_MB_DQS_H0 <<> MEM_MB_DQS_H0 7 DQS0
9,16 MEM_MB_DQS_L1 <<> MEM_MB_DQS_L1 15 DQS1-
9,16 MEM_MB_DQS_H1 <<> MEM_MB_DQS_H1 16 DQS1
9,16 MEM_MB_DQS_L2 <<> MEM_MB_DQS_L2 24 DQS2-
9,16 MEM_MB_DQS_H2 <<> MEM_MB_DQS_H2 25 DQS2
9,16 MEM_MB_DQS_L3 <<> MEM_MB_DQS_L3 33 DQS3-
9,16 MEM_MB_DQS_H3 <<> MEM_MB_DQS_H3 34 DQS3
9,16 MEM_MB_DQS_L4 <<> MEM_MB_DQS_L4 84 DQS4-
9,16 MEM_MB_DQS_H4 <<> MEM_MB_DQS_H4 85 DQS4
9,16 MEM_MB_DQS_L5 <<> MEM_MB_DQS_L5 93 DQS5-
9,16 MEM_MB_DQS_H5 <<> MEM_MB_DQS_H5 94 DQS5
9,16 MEM_MB_DQS_L6 <<> MEM_MB_DQS_L6 102 DQS6-
9,16 MEM_MB_DQS_H6 <<> MEM_MB_DQS_H6 103 DQS6
9,16 MEM_MB_DQS_L7 <<> MEM_MB_DQS_L7 111 DQS7-
9,16 MEM_MB_DQS_H7 <<> MEM_MB_DQS_H7 112 DQS7
9,16 MEM_MB_DQS_L8 <<> MEM_MB_DQS_L8 42 DQS8-
9,16 MEM_MB_DQS_H8 <<> MEM_MB_DQS_H8 43 DQS8

FOR ECC

9,16 MEM_MB_DM[7..0] <<>

MEM_MB_DM0 125 DM0/DQS9
MEM_MB_DM1 134 DQS9-
MEM_MB_DM2 135 DM1/DQS10
MEM_MB_DM3 143 DQS10-
MEM_MB_DM4 144 DM2/DQS11
MEM_MB_DM5 152 DQS11-
MEM_MB_DM6 153 DM3/DQS12
MEM_MB_DM7 203 DQS12-
MEM_MB_DM8 204 DM4/DQS13
MEM_MB_DM9 212 DQS13-
MEM_MB_DM10 221 DM5/DQS14
MEM_MB_DM11 222 DQS14-
MEM_MB_DM12 223 DM6/DQS15
MEM_MB_DM13 230 DQS15-
MEM_MB_DM14 231 DM7/DQS16
MEM_MB_DM15 161 DQS16-
MEM_MB_DM16 162 DM8/DQS17
MEM_MB_DM17 162 DQS17-

FOR ECC

9,16 MEM_MB_CHECK[7..0] <<>

MEM_MB_CHECK0 39 CB0
MEM_MB_CHECK1 40 CB1
MEM_MB_CHECK2 45 CB2
MEM_MB_CHECK3 46 CB3
MEM_MB_CHECK4 158 CB4
MEM_MB_CHECK5 159 CB5
MEM_MB_CHECK6 164 CB6
MEM_MB_CHECK7 165 CB7

FOR ECC

13,15,16,22,38,41 SDATA <<>
13,15,16,22,38,41 SCLK <<>

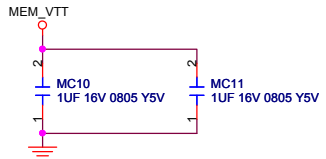
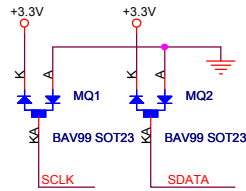
9,16 MEM_MB_ADD[15..0] <<>

MEM_MB_ADD0 188 A0
MEM_MB_ADD1 181 A1
MEM_MB_ADD2 61 A2
MEM_MB_ADD3 180 A3
MEM_MB_ADD4 59 A4
MEM_MB_ADD5 58 A5
MEM_MB_ADD6 178 A6
MEM_MB_ADD7 58 A7
MEM_MB_ADD8 177 A8
MEM_MB_ADD9 70 A9
MEM_MB_ADD10 55 A10
MEM_MB_ADD11 174 A11
MEM_MB_ADD12 196 A12
MEM_MB_ADD13 172 A13
MEM_MB_ADD14 172 A14
MEM_MB_ADD15 171 A15

BLACK

NC/PAR_IN
NC/ERR_OUT
NC/TEST4

DDR3-240 PIN-W



MEM_MB_DATA[63..0] 9,16

234 MEM_MB_DATA63
233 MEM_MB_DATA62
228 MEM_MB_DATA61
227 MEM_MB_DATA60
115 MEM_MB_DATA59
114 MEM_MB_DATA58
109 MEM_MB_DATA57
108 MEM_MB_DATA56
225 MEM_MB_DATA55
224 MEM_MB_DATA54
219 MEM_MB_DATA53
218 MEM_MB_DATA52
106 MEM_MB_DATA51
105 MEM_MB_DATA50
100 MEM_MB_DATA49
99 MEM_MB_DATA48
216 MEM_MB_DATA47
215 MEM_MB_DATA46
210 MEM_MB_DATA45
209 MEM_MB_DATA44
97 MEM_MB_DATA43
96 MEM_MB_DATA42
91 MEM_MB_DATA41
90 MEM_MB_DATA40
207 MEM_MB_DATA39
206 MEM_MB_DATA38
201 MEM_MB_DATA37
200 MEM_MB_DATA36
88 MEM_MB_DATA35
87 MEM_MB_DATA34
82 MEM_MB_DATA33
81 MEM_MB_DATA32
30 MEM_MB_DATA31
156 MEM_MB_DATA30
155 MEM_MB_DATA29
150 MEM_MB_DATA28
149 MEM_MB_DATA27
37 MEM_MB_DATA26
36 MEM_MB_DATA25
31 MEM_MB_DATA24
30 MEM_MB_DATA23
147 MEM_MB_DATA22
146 MEM_MB_DATA21
141 MEM_MB_DATA20
140 MEM_MB_DATA19
28 MEM_MB_DATA18
27 MEM_MB_DATA17
22 MEM_MB_DATA16
21 MEM_MB_DATA15
138 MEM_MB_DATA14
137 MEM_MB_DATA13
132 MEM_MB_DATA12
131 MEM_MB_DATA11
19 MEM_MB_DATA10
18 MEM_MB_DATA9
13 MEM_MB_DATA8
12 MEM_MB_DATA7
128 MEM_MB_DATA6
123 MEM_MB_DATA5
122 MEM_MB_DATA4
10 MEM_MB_DATA3
9 MEM_MB_DATA2
4 MEM_MB_DATA1
3 MEM_MB_DATA0

APU_VDDIO_SUS

DDR3_B1B

51 VDDQ1 (P)
54 VDDQ2 (P)
57 VDDQ3 (P)
60 VDDQ4 (P)
62 VDDQ5 (P)
65 VDDQ6 (P)
66 VDDQ7 (P)
72 VDDQ8 (P)
75 VDDQ9 (P)
78 VDDQ10 (P)
79 VDDQ11 (P)
170 VDD1 (P)
173 VDD2 (P)
176 VDD3 (P)
179 VDD4 (P)
182 VDD5 (P)
183 VDD6 (P)
186 VDD7 (P)
189 VDD8 (P)
191 VDD9 (P)
194 VDD10 (P)
197 VDD11 (P)
236 VDDSPD (P)

+3.3V

DIMM_CA_VREF

DIMM_DQ_VREF

+3.3V

SA0

SA1

CKE0

CKE1

BA0

BA1

A16/BA2

RESET

WE-

RAS-

CAS-

S-0

S-1

ODT0

ODT1

CK-1

CK1

CK-0

CK0

FREE1

FREE2

FREE3

FREE4

DDR3-240 PIN-W

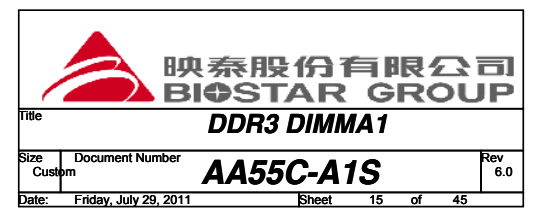
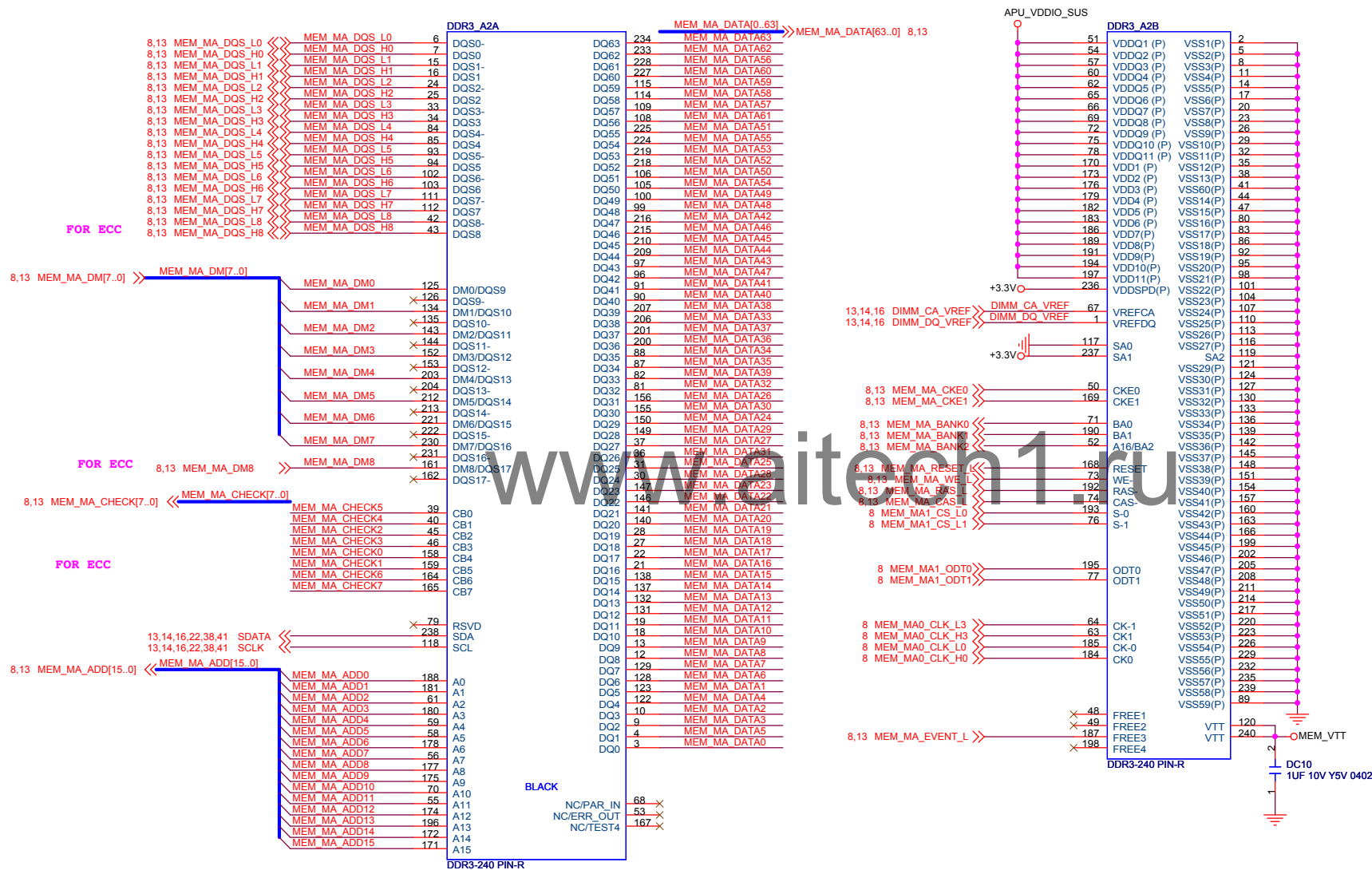
映泰股份有限公司
BIOSTAR GROUP

Title: **DDR DIMM-2**

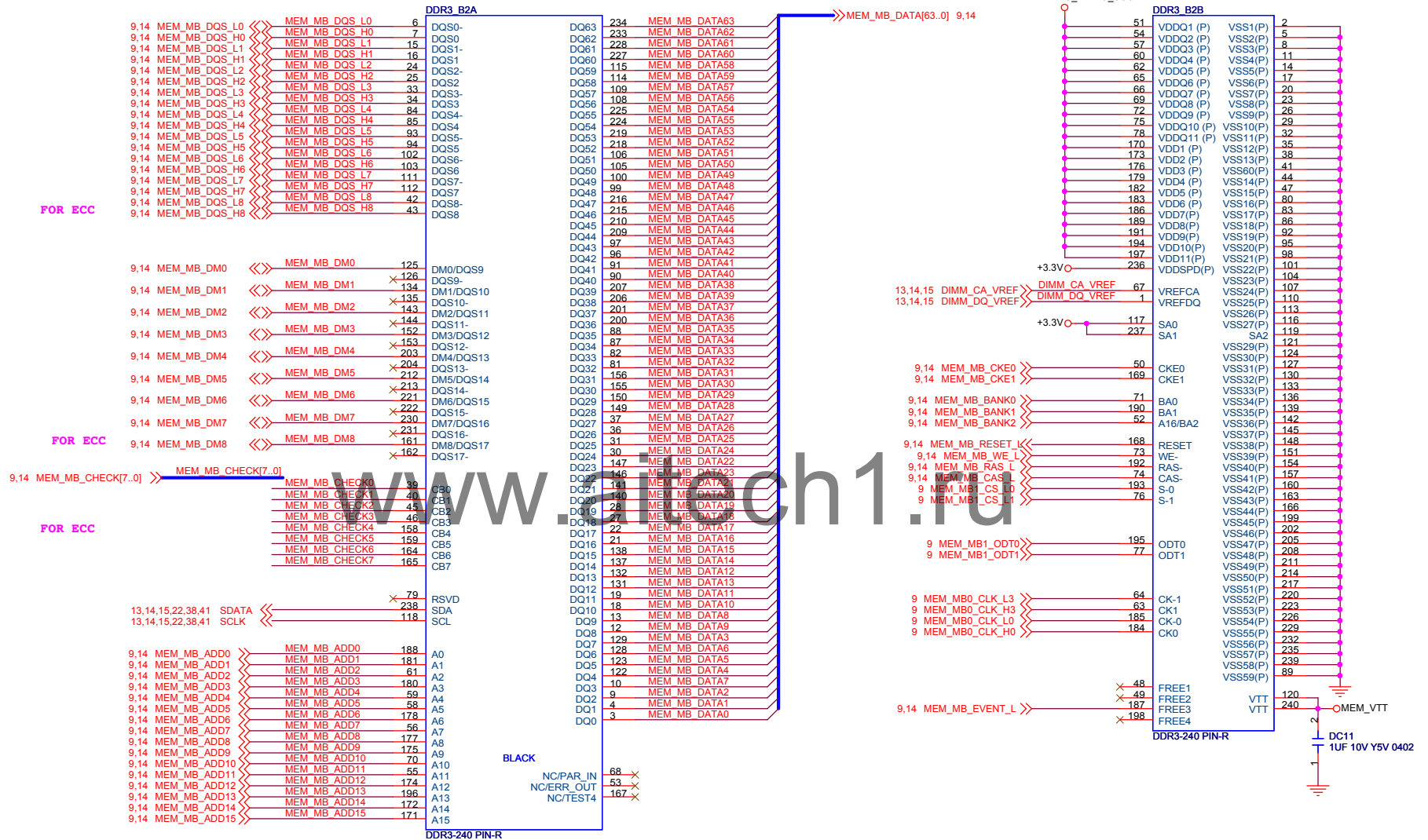
Size: Custom Document Number: **AA55C-A1S** Rev: 6.0

Date: Friday, July 29, 2011 Sheet: 14 of 45

DDR3_A2

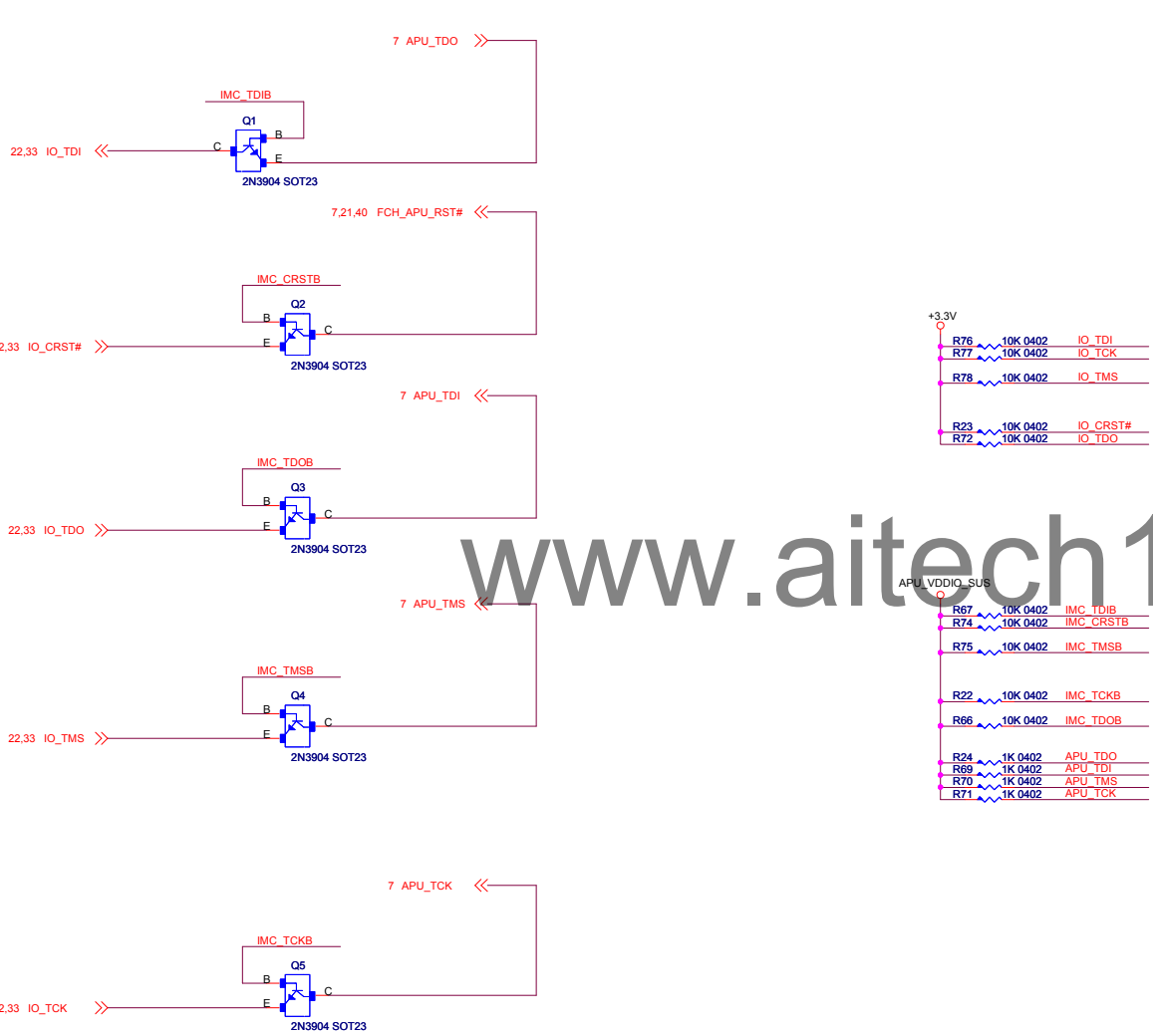


DDR3_B2



Title: DDR3 DIMMB1	
Size: Custom	Document Number: AA55C-A1S
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5 4 3 2 1



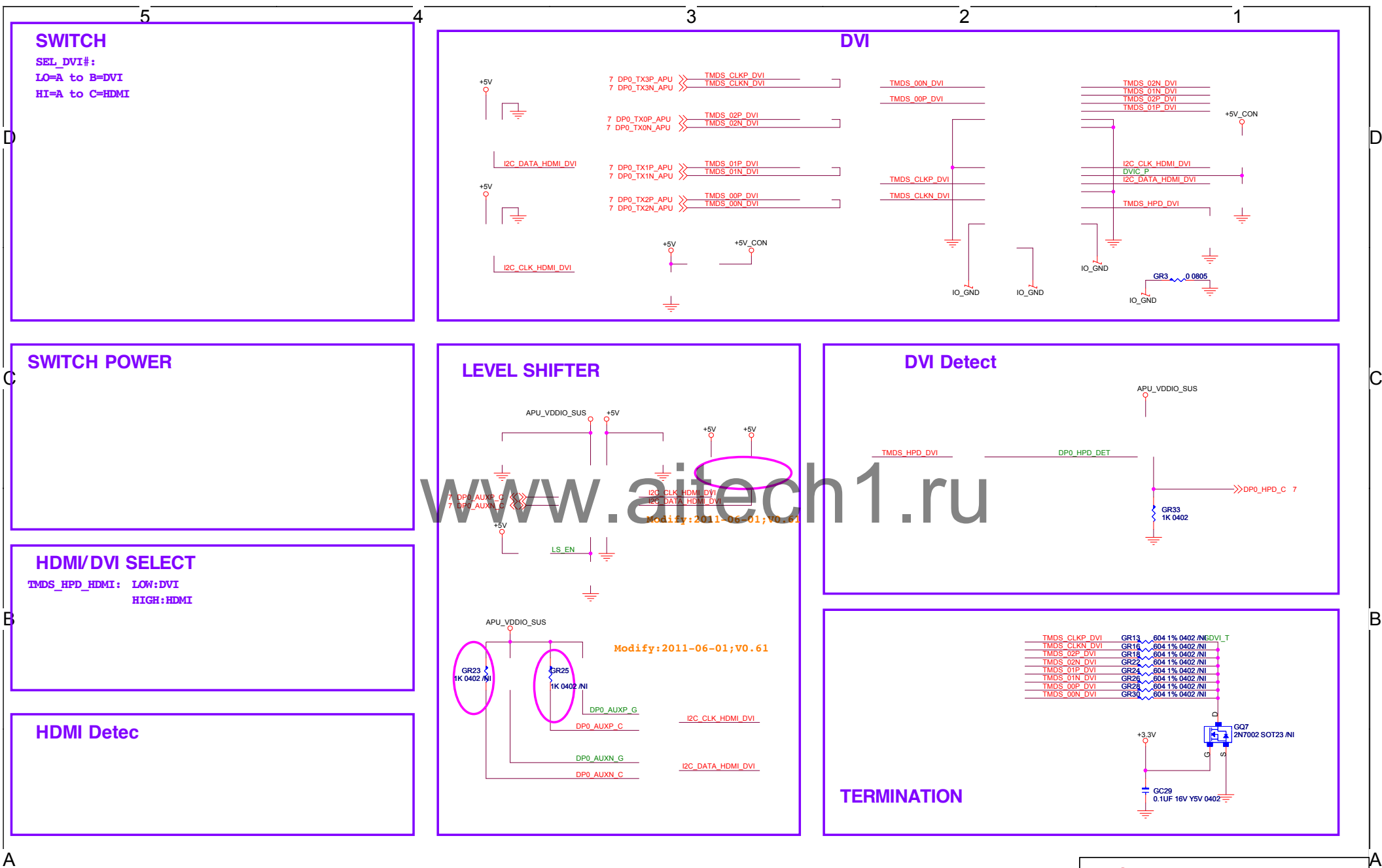
www.aitech1.ru

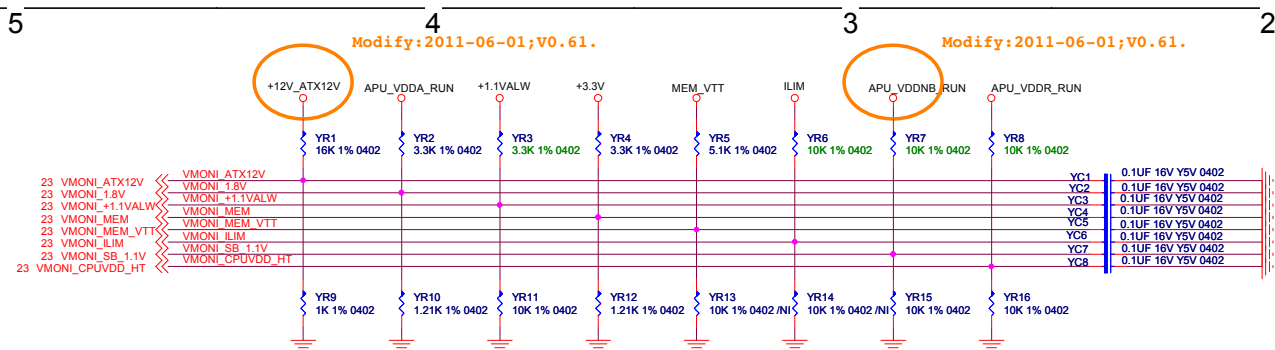


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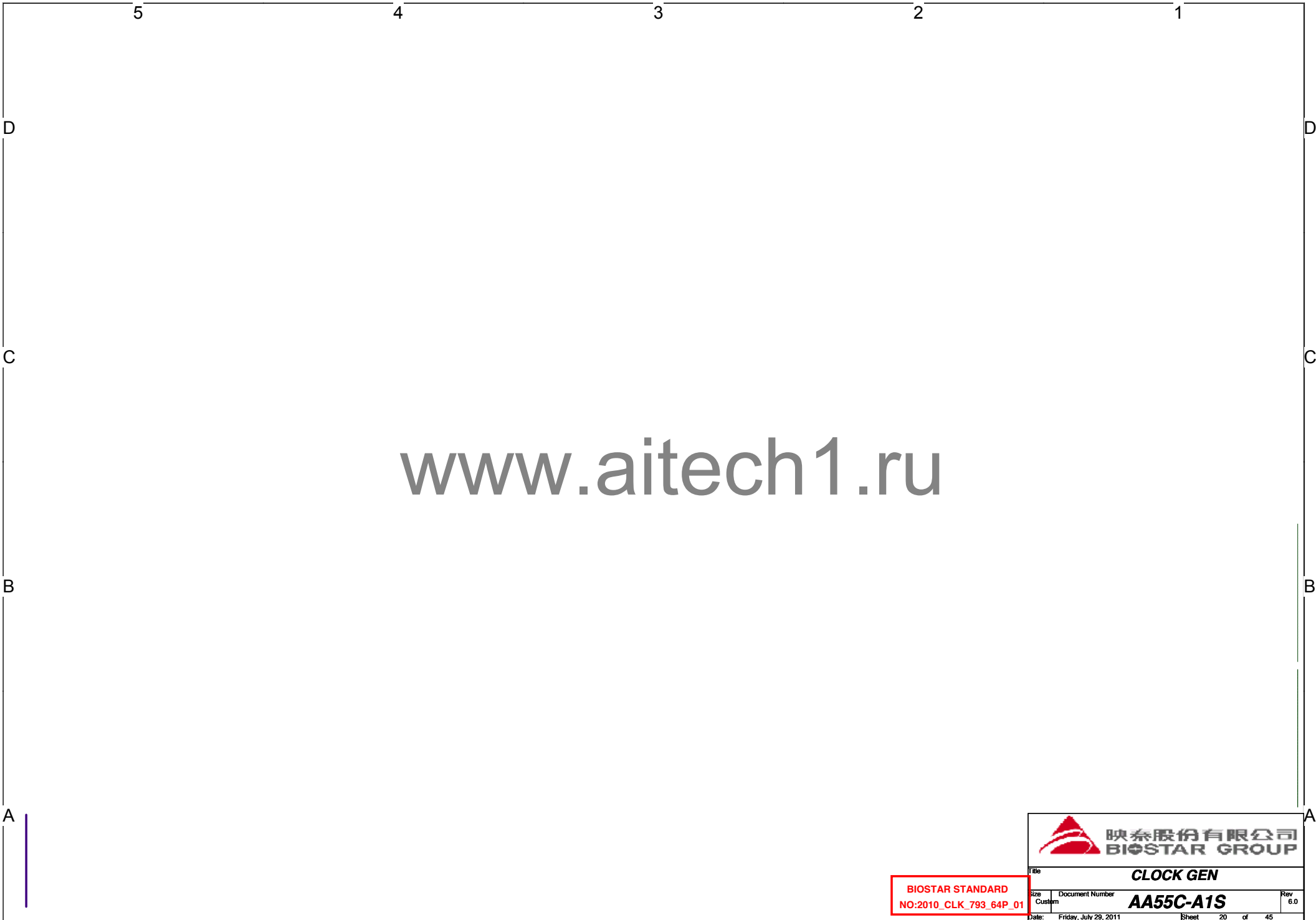
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Size	Document Number		AA55C-A1S		Rev
Custom					6.0
Date	Friday, July 29, 2011		Sheet	17	of 45





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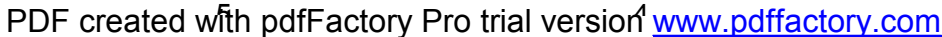
			
SB HW MONITOR			
Size	Document Number	Rev	
Custom	AA55C-A1S	6.0	
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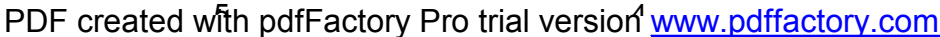


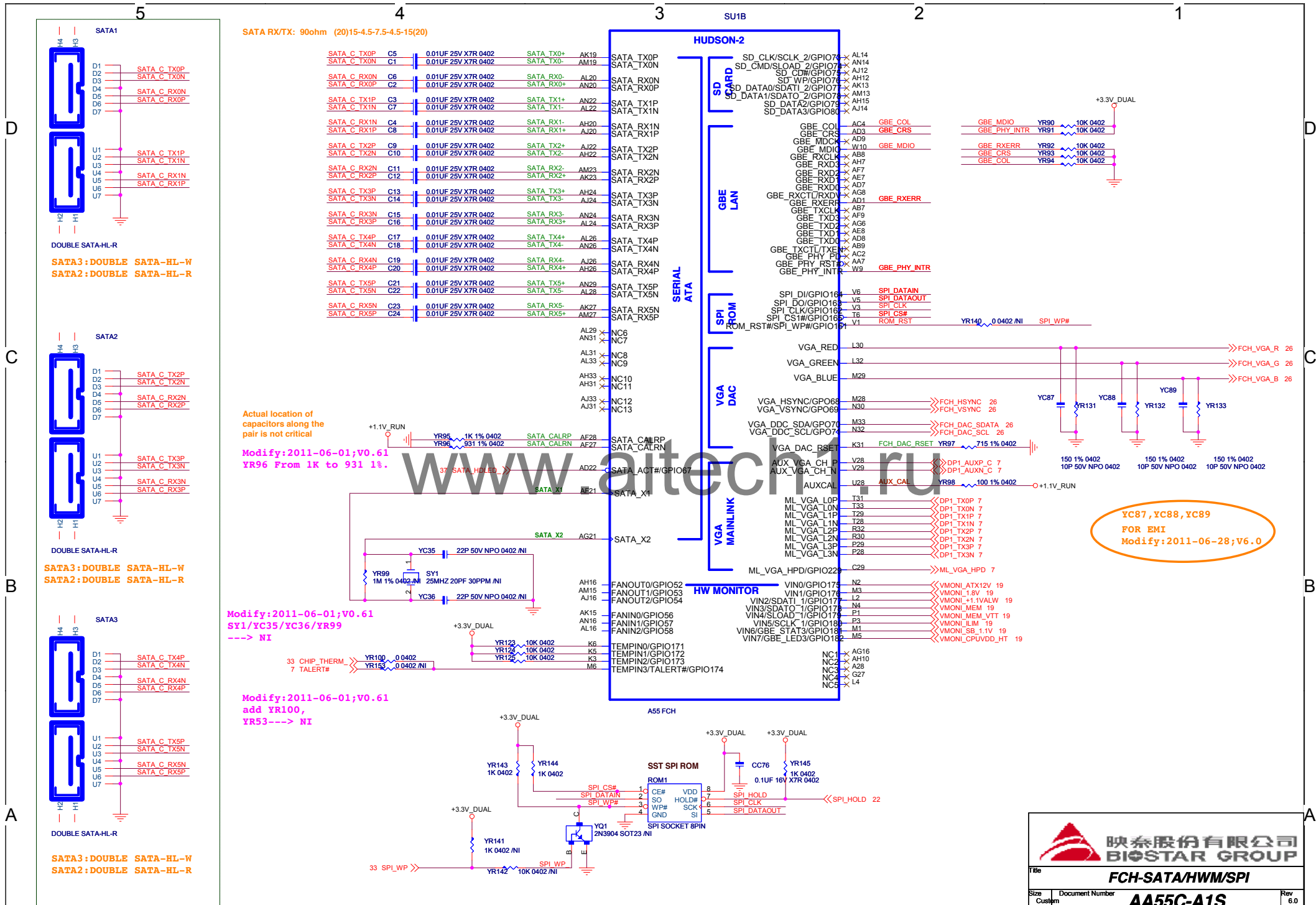
www.aitech1.ru

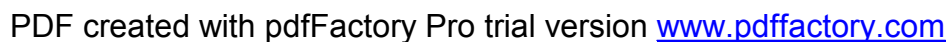
BIOSTAR STANDARD
NO:2010_CLK_793_64P_01

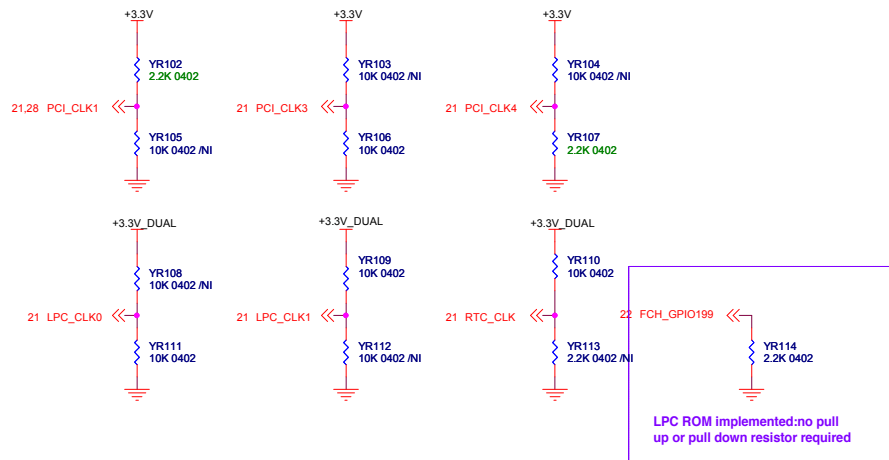
		映泰股份有限公司 BIOSTAR GROUP	
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Size	Document Number	AA55C-A1S	Rev
Custom			6.0
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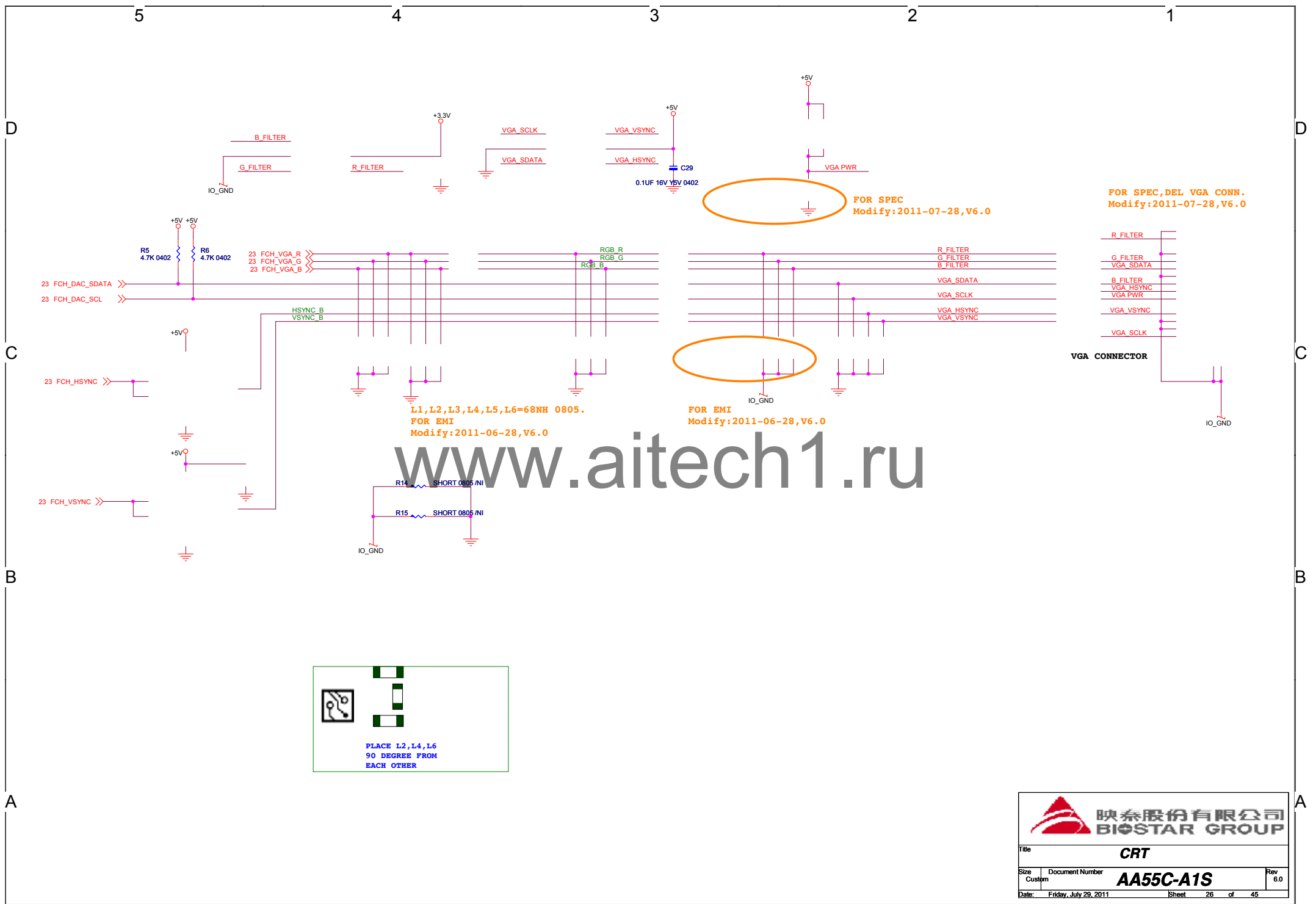


REQUIRED STRAPS

	RTC_CLK	PCI_CLK1	PCI_CLK3	PCI_CLK4	LPC_CLK0	LPC_CLK1	GPIO199
PULL HIGH	S5+ DISABLE DEFAULT	ALLOW PCIE GEN2 DEFAULT	USE DEBUG STRAPS	NON-FUSION CPU CLOCK MODE	EC ENABLED	CLKGEN ENABLED DEFAULT	ROM TYPE: H=LPC ROM
PULL LOW	S5+ ENABLE	FORCE PCIE GEN1	IGNORE DEBUG STRAPS DEFAULT	FUSION CPU CLOCK MODE DEFAULT	EC DISABLED DEFAULT	CLKGEN DISABLED	L = SPI ROM DEFAULT

NOTE: HUDSON-D1 HAS INTERNAL 15K PULL UP RESISTOR FOR PCI_AD[30:23]

 映泰股份有限公司 BIOSSTAR GROUP		
Title FCH-STRAPS		
Size Custom	Document Number AA55C-A1S	Rev 6.0
Date: Friday, July 29, 2011	Sheet 25 of 45	1

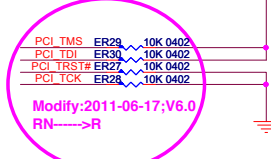
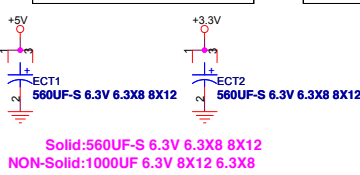
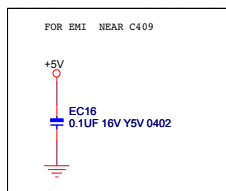
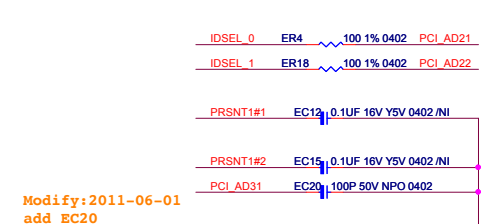
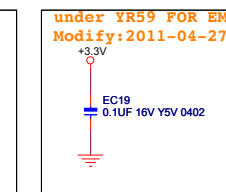
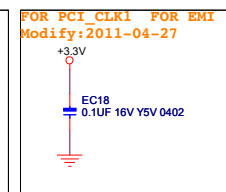
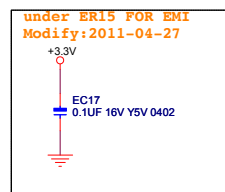
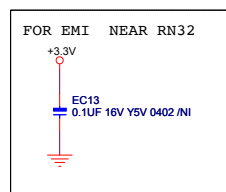
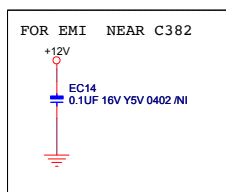
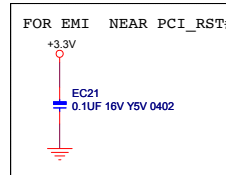
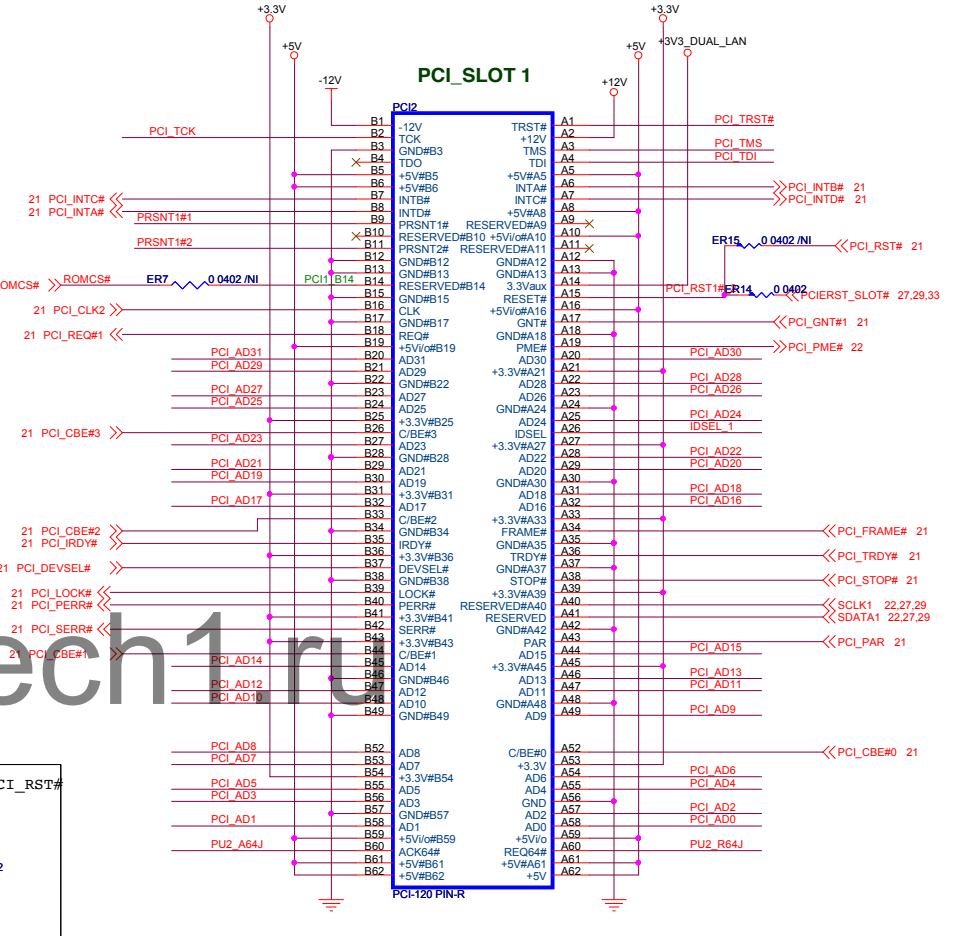
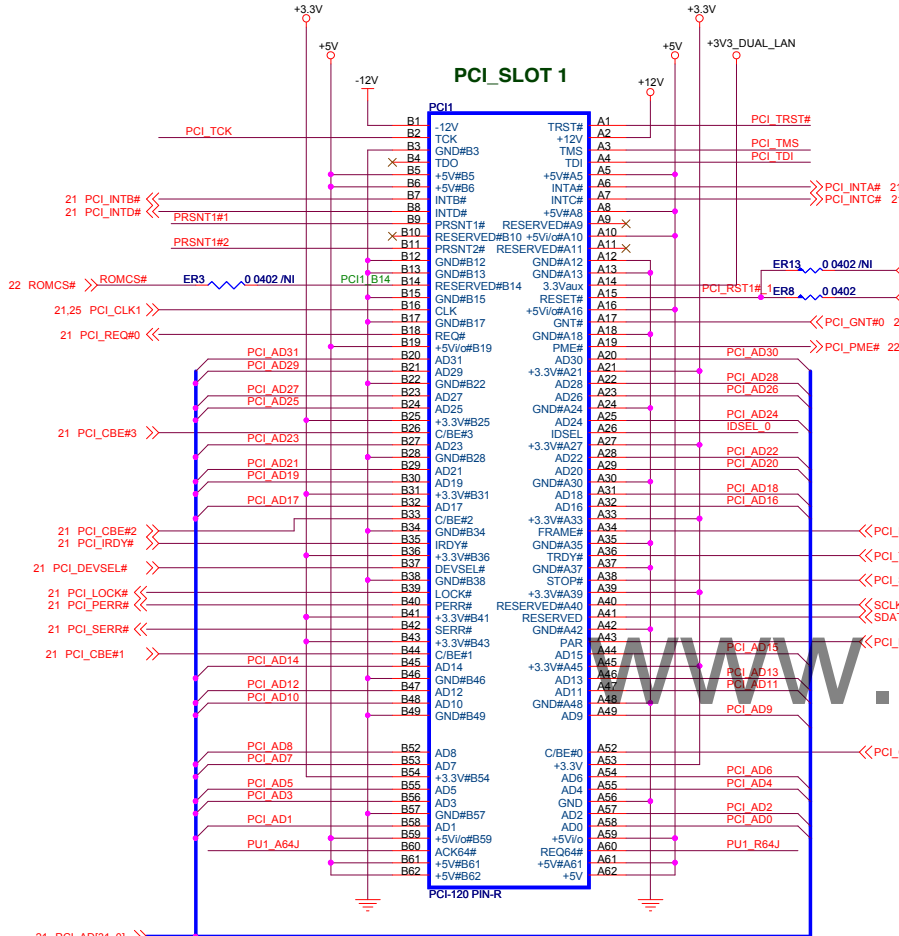


IDSEL:AD21, INT:ABCD, REQ0 & GNT0, PCI_CLK3

IDSEL:AD22, INT:BCDA, REQ0 & GNT0, PCI_CLK2

PCI_SLOT 1

PCI_SLOT 1

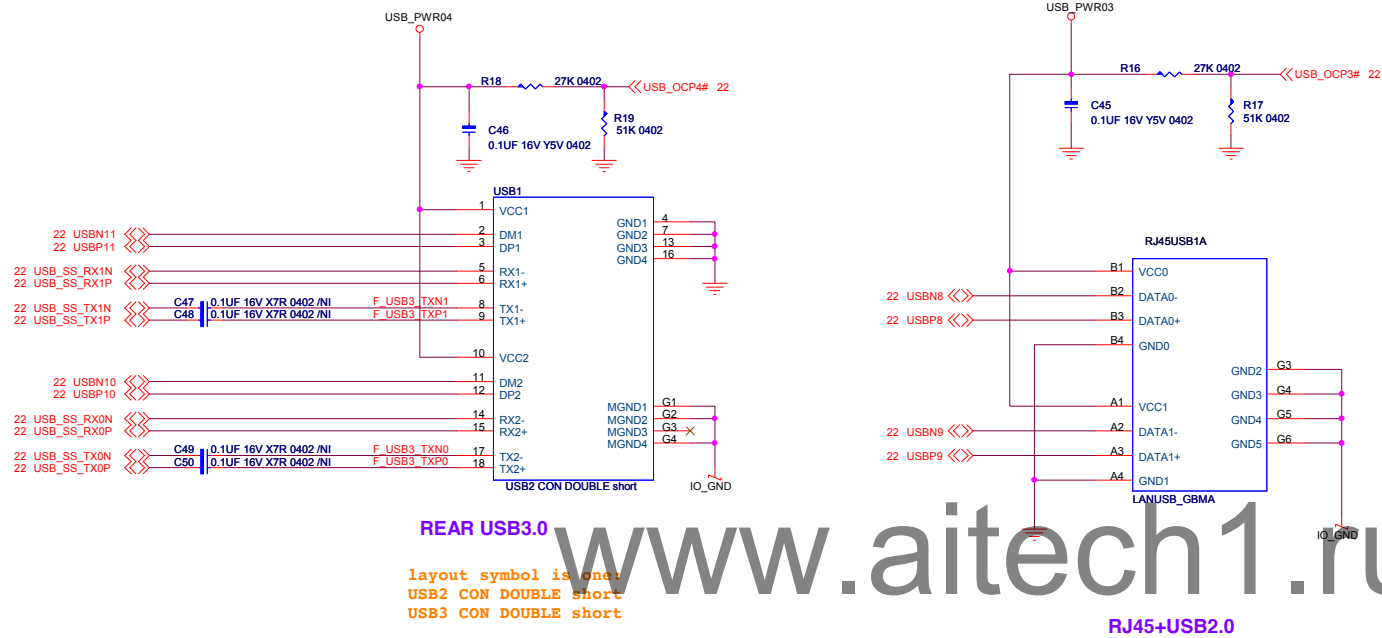


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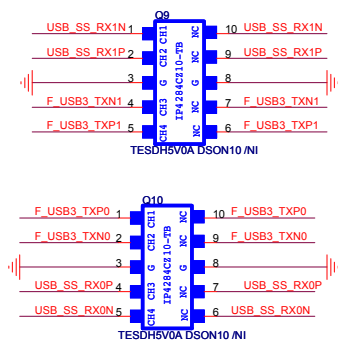
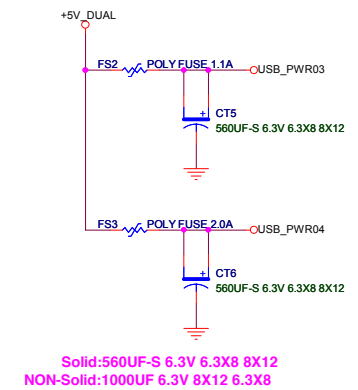
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Size: Custom Document Number: **AA55C-A1S** Rev: 6.0

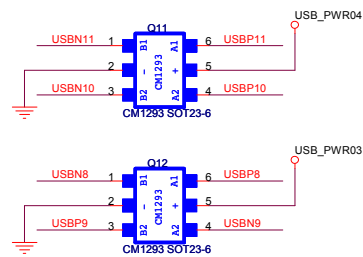
Date: Friday, July 29, 2011 Sheet: 28 of 45



REAR USB POWER



REAR USB ESD

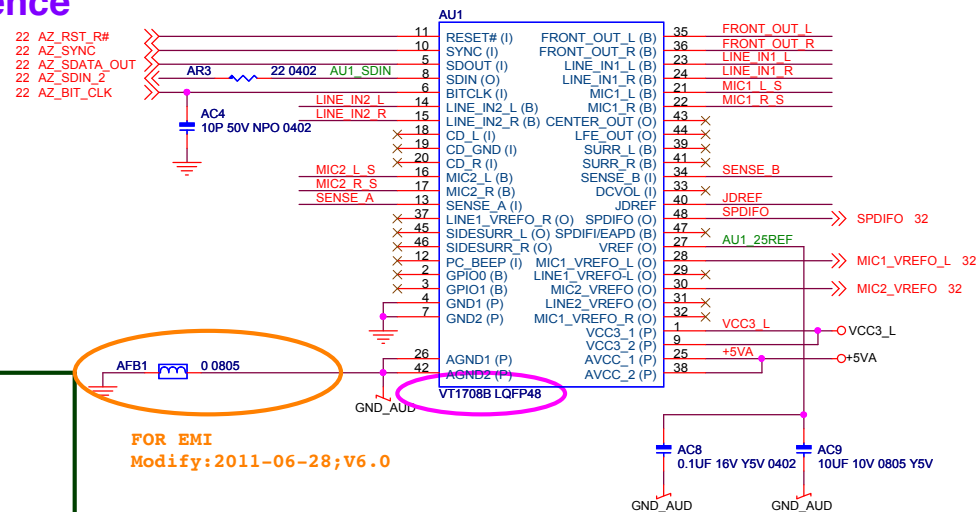
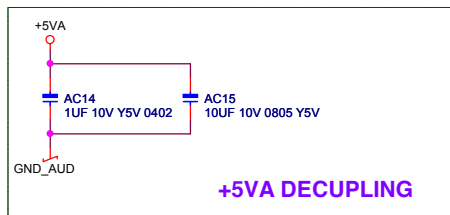
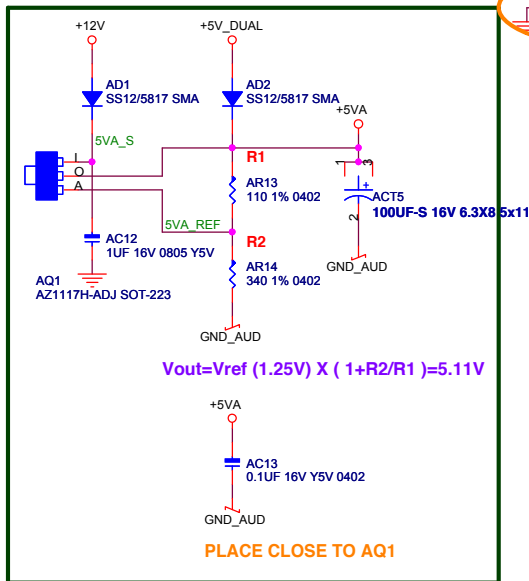


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BIOSSTAR GROUP

Title: **USB CONN**

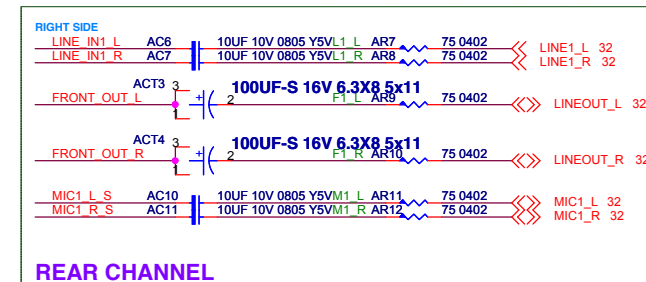
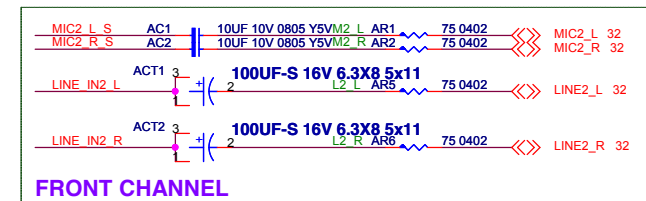
Size: Custom Document Number: **AA55C-A1S** Rev: 6.0

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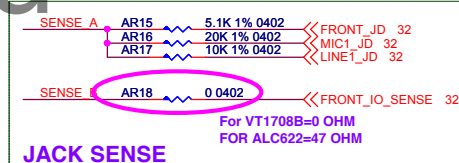


FOR EMI
Modify:2011-06-28;V6.0

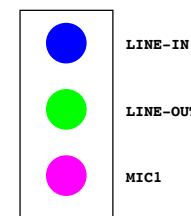
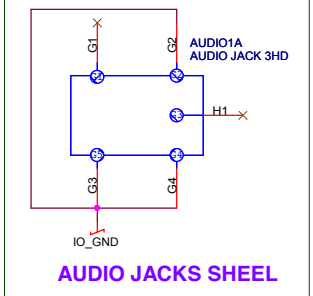
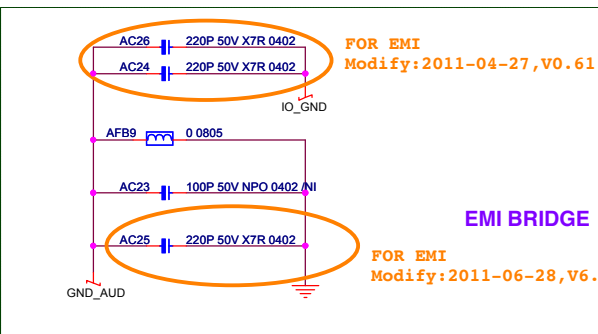
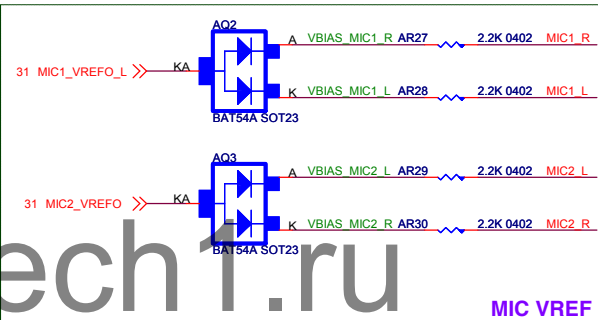
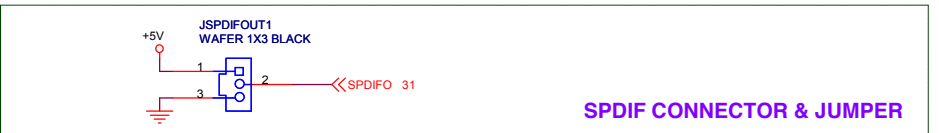
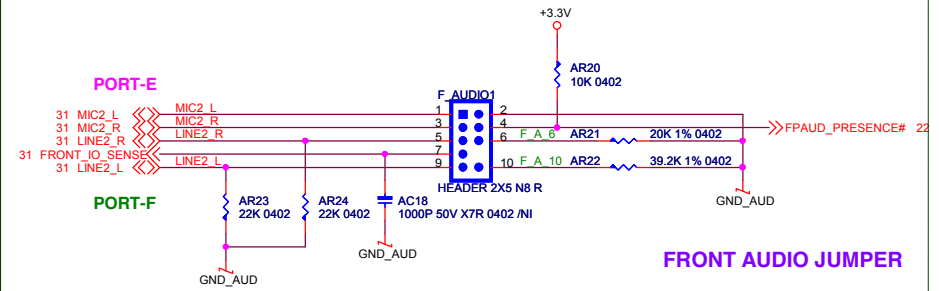
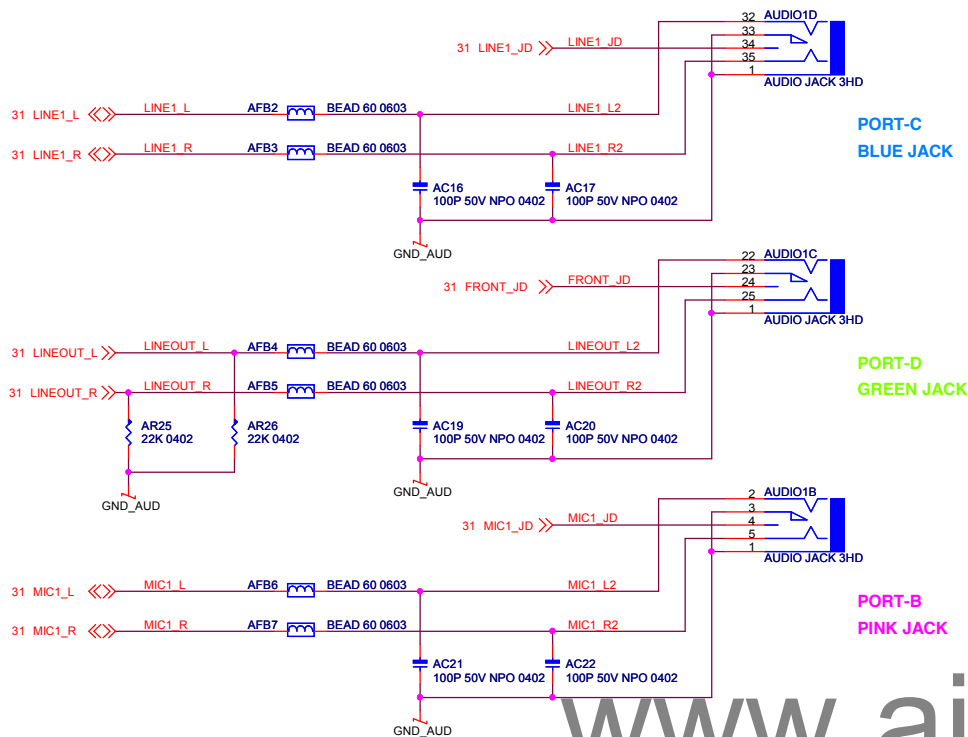
Solid:100UF-S 16V 6.3X8 5x11
NON-Solid:100UF 16V 5X11 2mm LR 6.3X5



CD IN CONNECTOR



Title			
CODEC ALC 662			
Size B	Document Number		Rev 6
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Title			
AUDIO CONNECTOR			
Size	Document Number	Rev	
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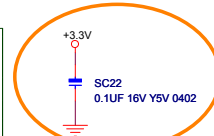
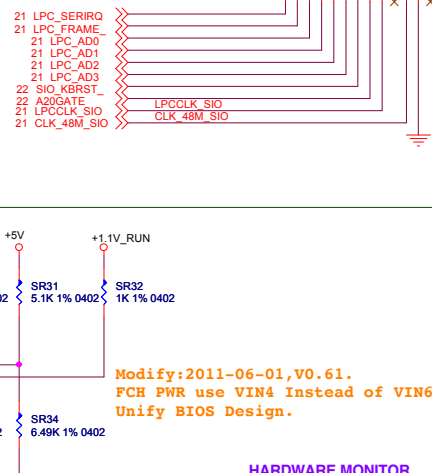
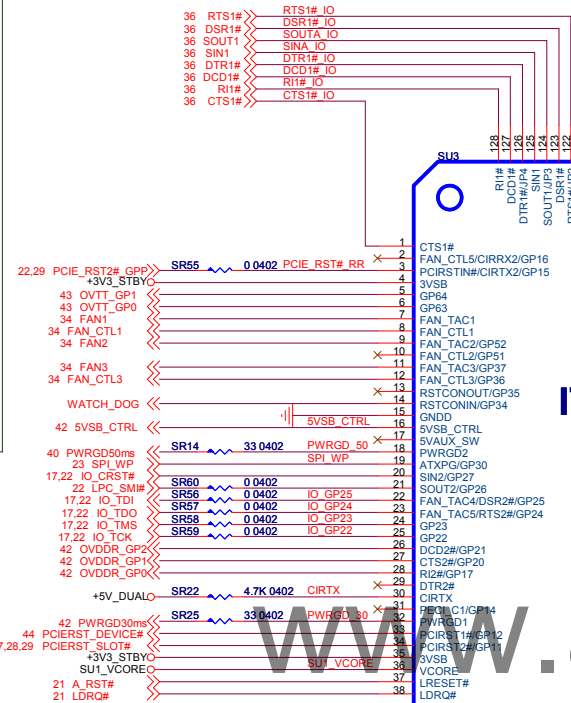
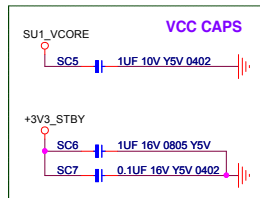
Diagram illustrating the SuperIO Pulls configuration for the T1020. The diagram shows connections for various pins (SR2 through SR11) to ground or power rails (+3.3V, +3V3_STBY, +3.3V_DUAL) using pull-up resistors (4.7K 0402 or 1K 0402).

Pin Connections:

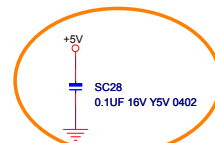
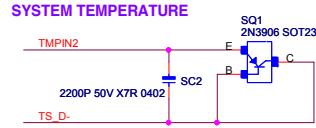
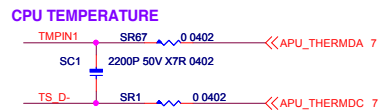
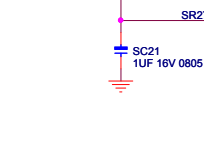
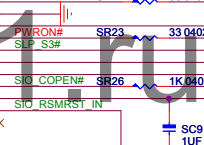
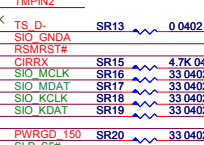
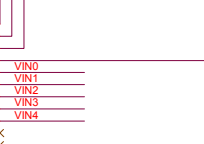
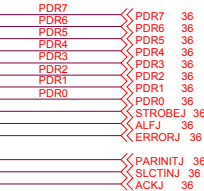
- SR2:** Connected to +3.3V via a 4.7K 0402 resistor. Functions: DTR1# IO JP4, SOUTA IO JP3.
- SR3:** Connected to +3.3V via a 1K 0402 resistor. Functions: PCIE_RST# RR, PWRGD 30.
- SR4:** Connected to +3.3V via a 1K 0402 resistor. Functions: PWRGD 150, SPI_WP.
- SR5:** Connected to +3.3V via a 1K 0402 resistor. Functions: LPC_FRAME, 5VSB_CTRL.
- SR6:** Connected to +3.3V via a 4.7K 0402 resistor. Functions: PWRON# JP8, R11# IO.
- SR7:** Connected to +3.3V via a 4.7K 0402 resistor. Functions: RSMRST#.
- SR8:** Connected to +3.3V via a 4.7K 0402 resistor. Functions: RSMRST#.
- SR9:** Connected to +3.3V via a 1K 0402 resistor. Functions: RSMRST#.
- SR10:** Connected to +3.3V via a 4.7K 0402 resistor. Functions: RSMRST#.
- SR11:** Connected to +3.3V via a 1K 0402 resistor. Functions: RSMRST#.

Legend:

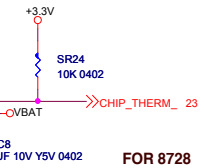
- 4.7K 0402:** Resistor value and package size.
- 1K 0402:** Resistor value and package size.
- PCIE_RST# RR:** Pin function and signal type (Active Low).
- PWRGD 30:** Pin function and signal type (Active Low).
- PWRGD 150:** Pin function and signal type (Active Low).
- SPI_WP:** Pin function and signal type (Active Low).
- LPC_FRAME:** Pin function and signal type (Active Low).
- 5VSB_CTRL:** Pin function and signal type (Active Low).
- PWRON# JP8:** Pin function, signal type (Active Low), and connector pin.
- R11# IO:** Pin function and signal type (Active Low).
- RSMRST#:** Pin function and signal type (Active Low).



FOR EMI
FOR CLK_48M_SIO
Modify:2011-06-28;V6.0



FOR EMI
close to SFB1.
Modify:2011-06-28;V6.0



FOR 8728

```
Modify:2011-06-01;V0.61
add SC21---->NI
T14 OK,SC21 NI
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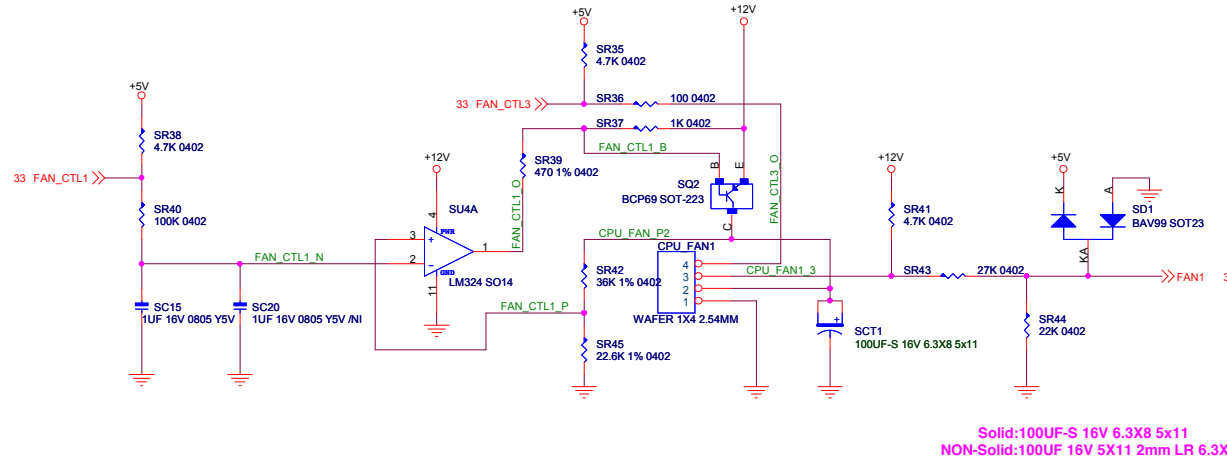
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◇Any unauthorized use, reproduction, duplication, or disclosure of this document will be subject to the applicable civil and/or criminal penalties.◆

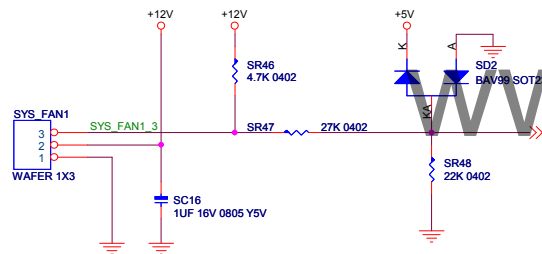


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Size	Document Number					Rev	
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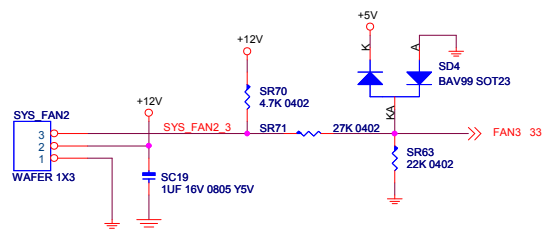
CPU FAN CONTROL



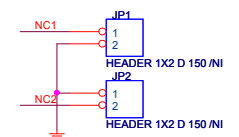
SYSTEM1 FAN



SYSTEM2 FAN




5 mil 60 ohm

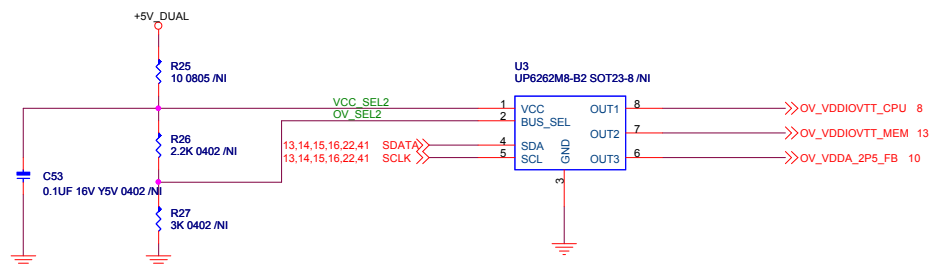


Title FAN CONTROL	
Size Custom	Document Number AA55C-A1S
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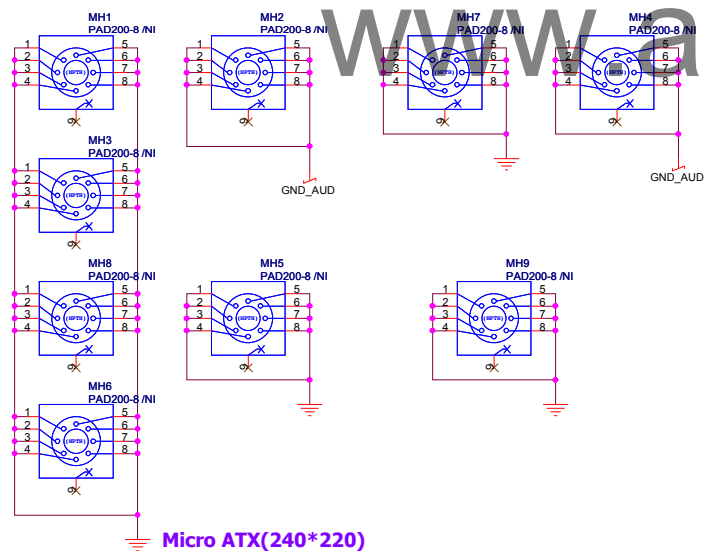
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		映泰股份有限公司 BIOSTAR GROUP	
Title RESERVE			
Size Custom	Document Number AA55C-A1S		Rev 6.0
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6262 OVER VOLTAGE IC

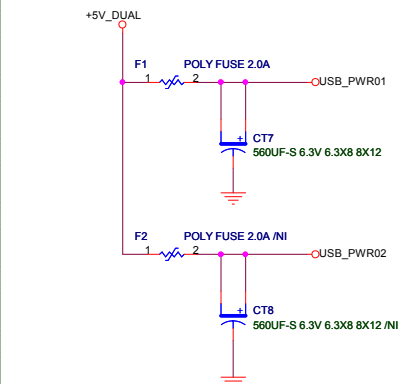


Micro ATX(240*220)

MT

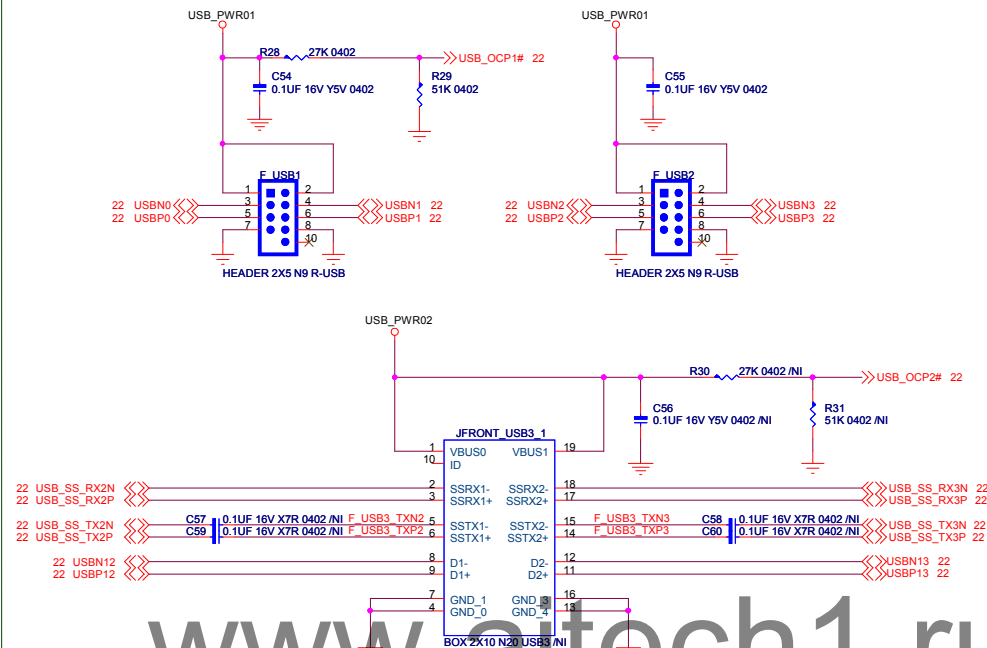
 映泰股份有限公司 BIOSSTAR GROUP			
Title OVER VOLTAGE			
Size Custom	Document Number AA55C-A1S		Rev 6.0
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FRONT USB POWER

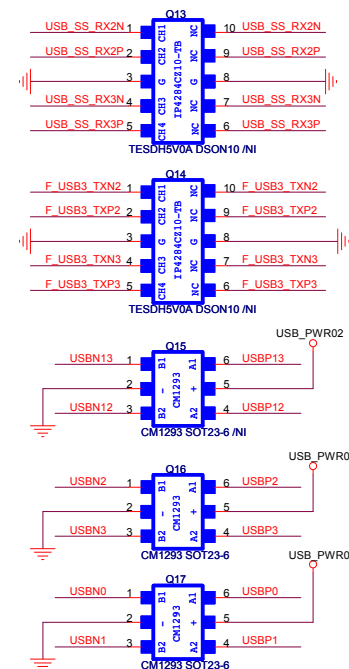


Solid:560UF-S 6.3V 6.3X8 8X12
NON-Solid:1000UF 6.3V 8X12 6.3X8

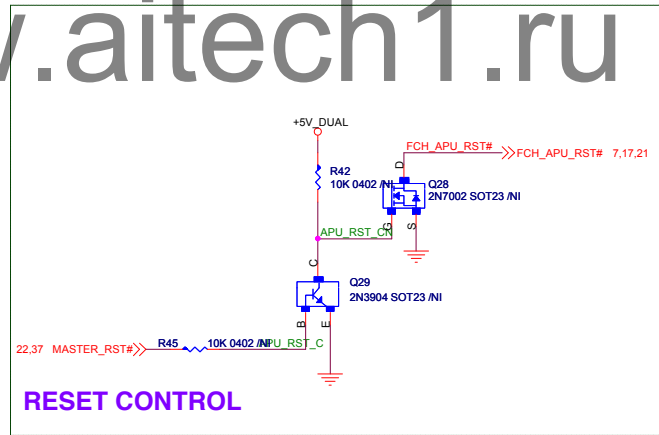
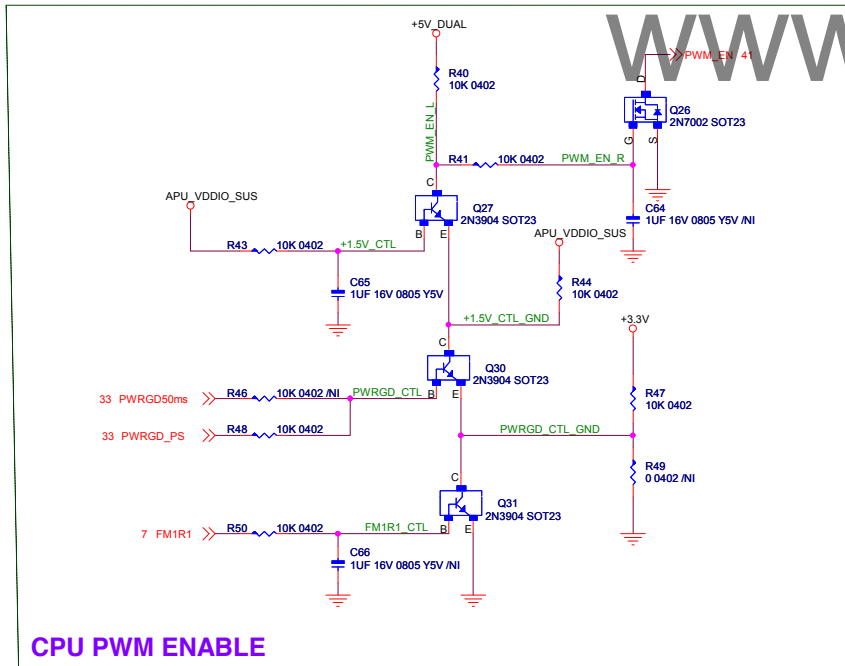
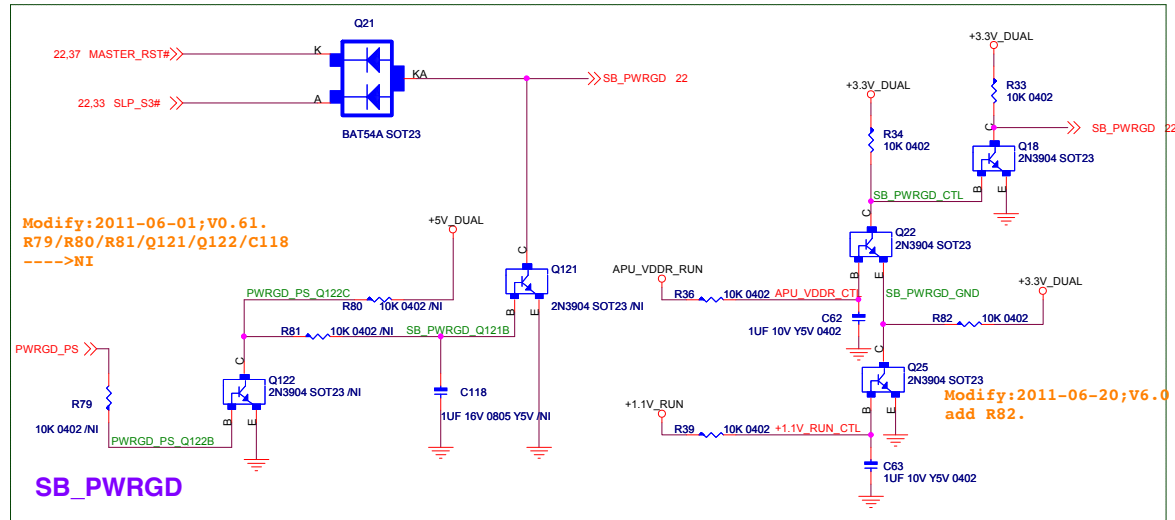
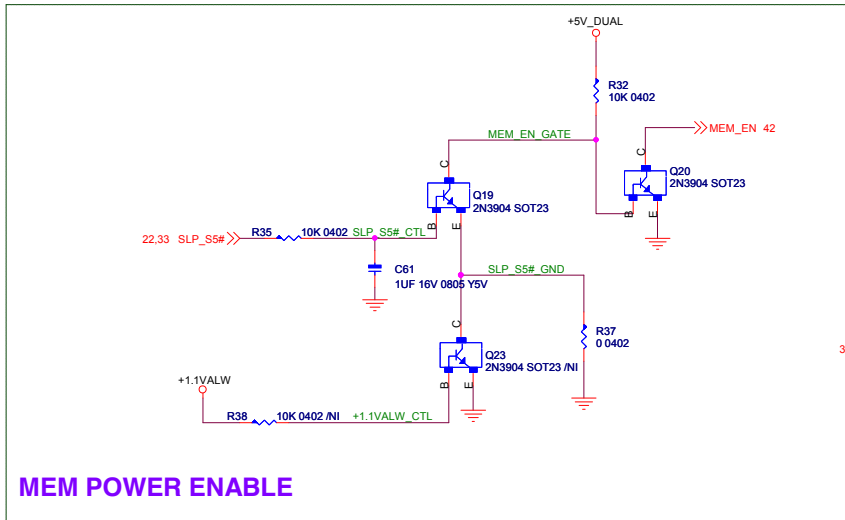
For T-Series-----560UF-S 6.3V 6.3X8 ELITE
For NO T-Series-----1000UF 6.3V 8X12
Layout Value:1000UF 6.3V 6.3X8 8X12
new colay value:(default=ELITE)
560UF-S 6.3V 6.3X8 8X12



FRONT USB HEADER

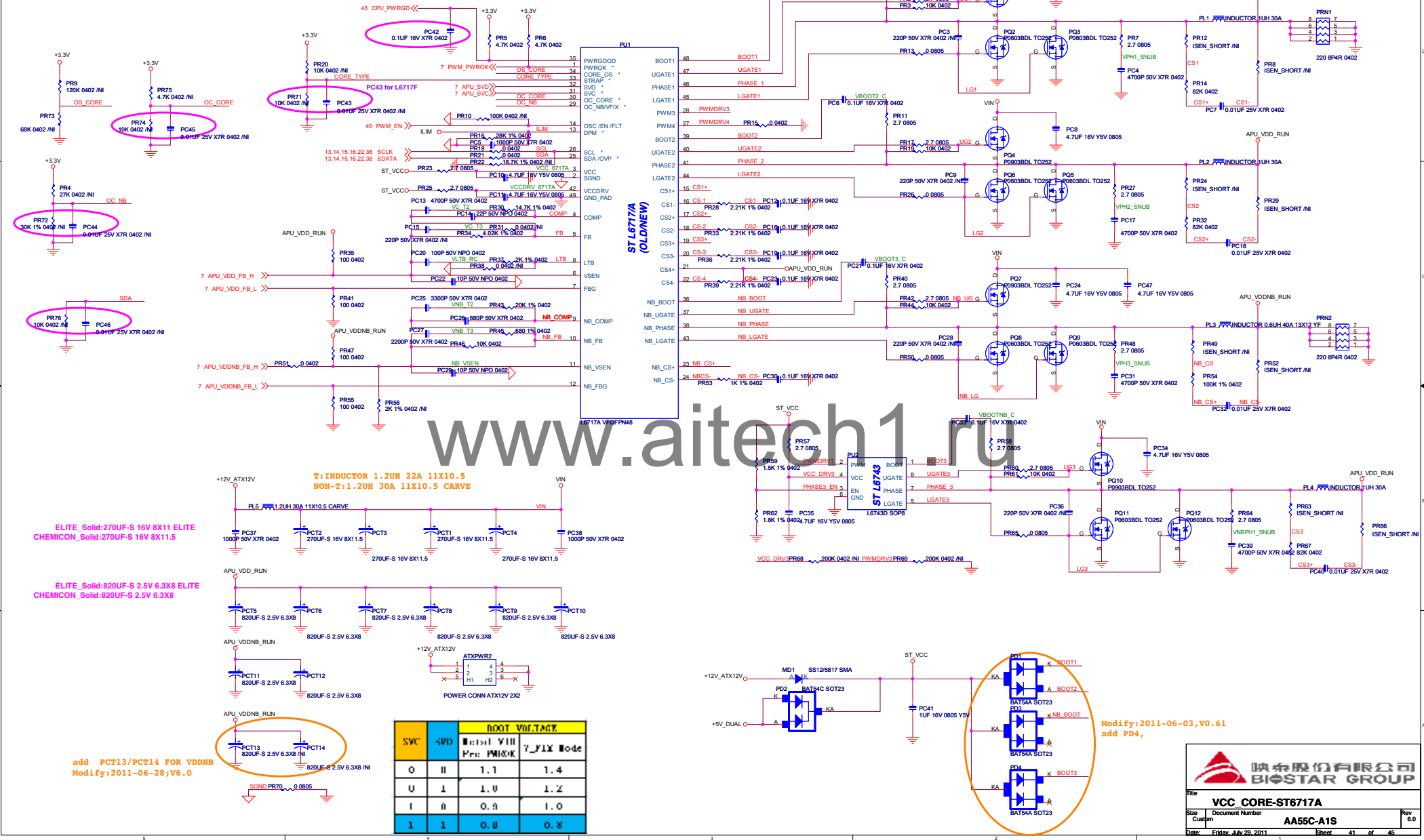


FRONT USB ESD



File PWR GD / MISC POWER			
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follow TW FM1 circuit;
2011-05-20

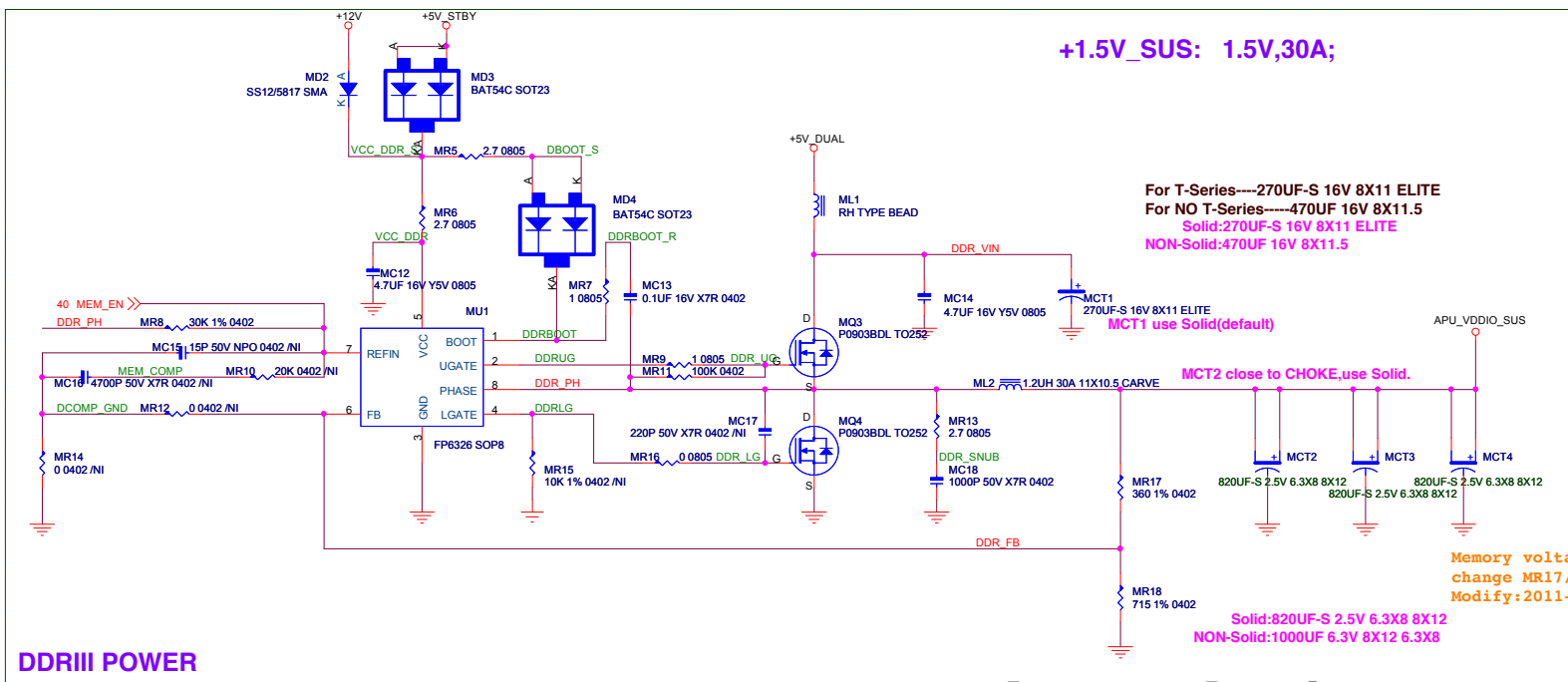


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BISTAR GROUP

Title: **VCC CORE-ST6717A**

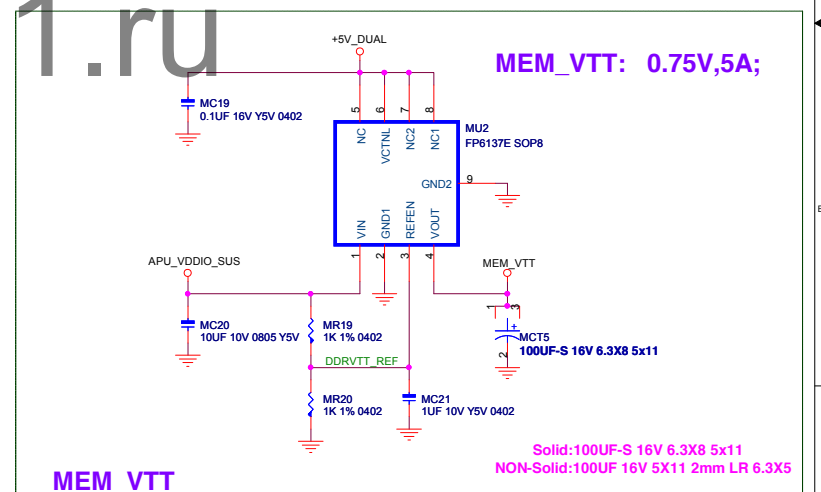
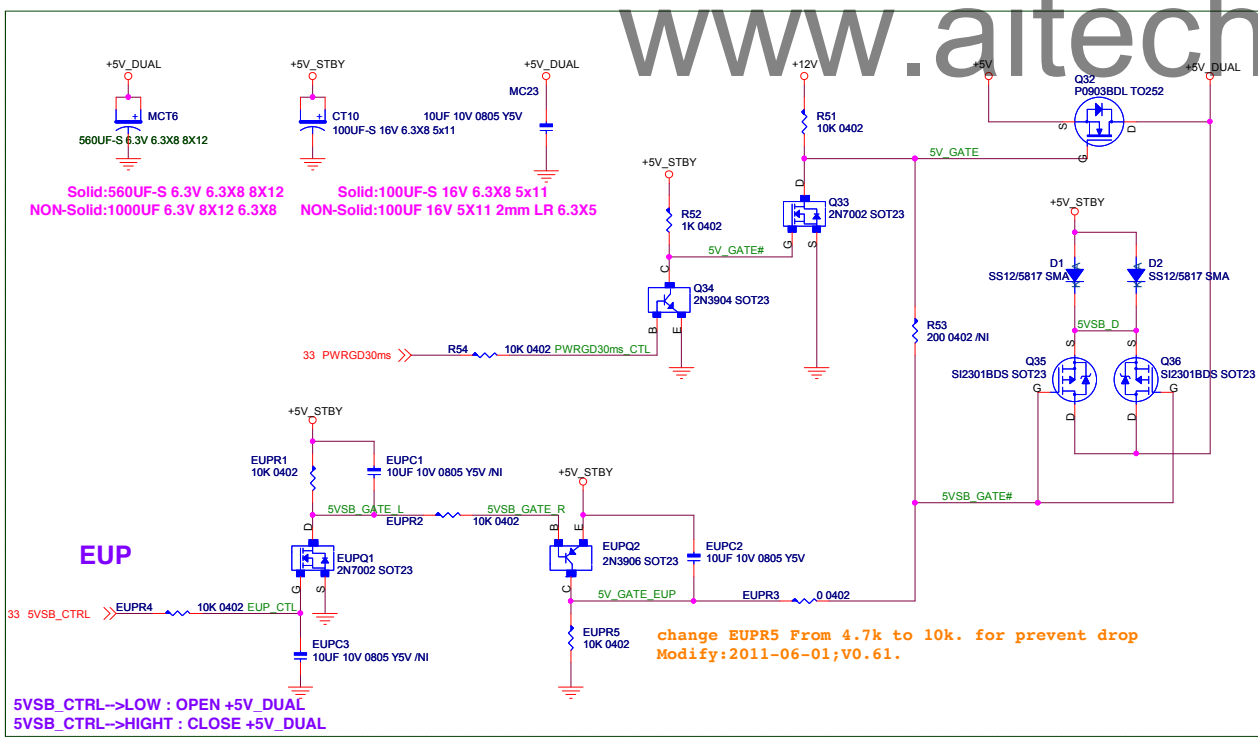
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GP2	GP1	GP0	APU_VDDIO_SUS
0	1	1	1.2V
0	1	0	1.3V
0	0	1	1.4V
0	0	0	1.5V
1	1	1	1.60V Default
1	1	0	1.7V
1	0	1	1.8V
1	0	0	1.9V

OV TABLE

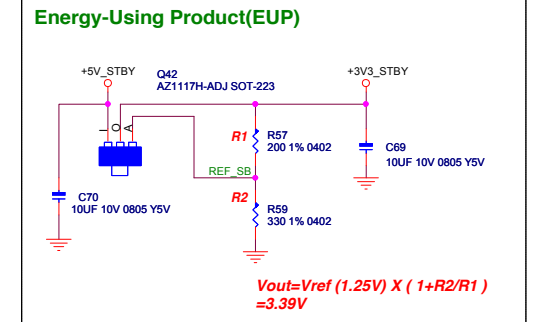
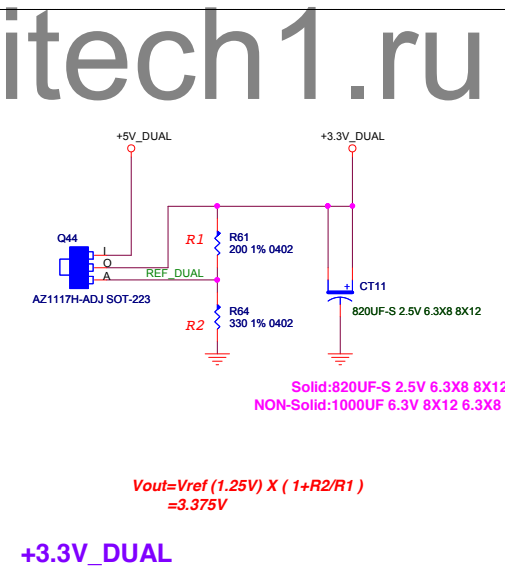
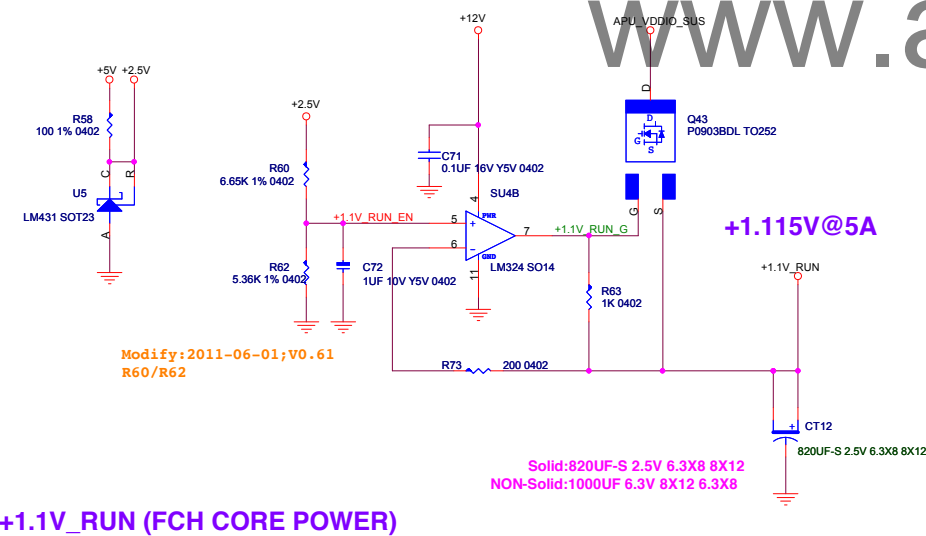
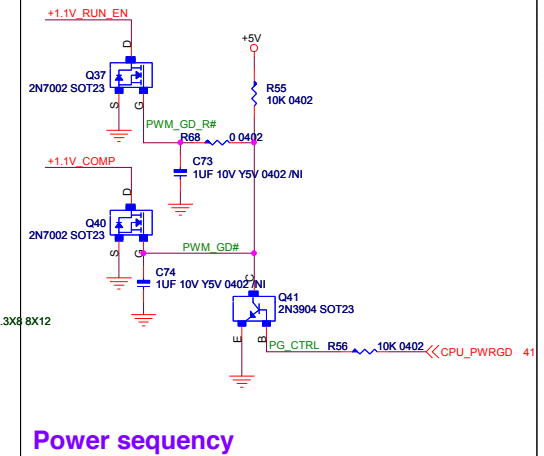
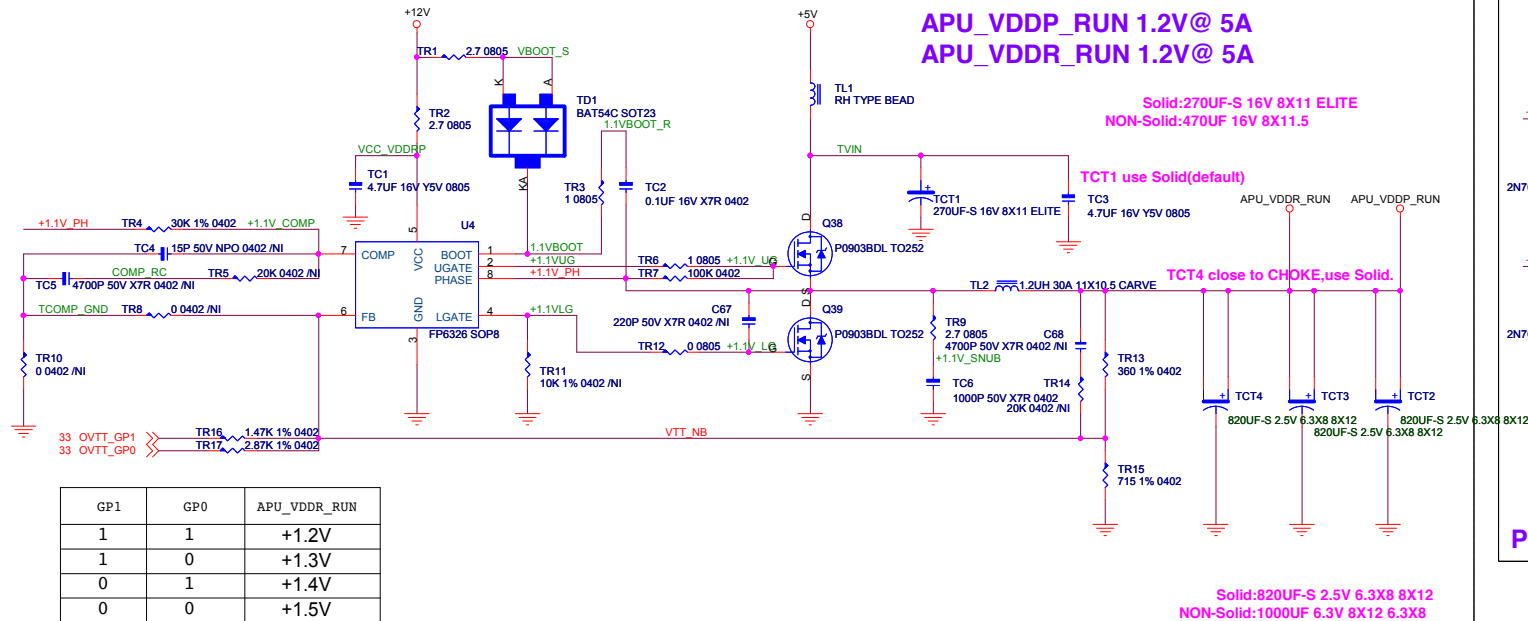


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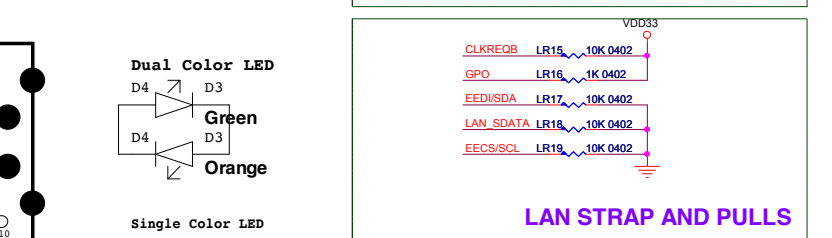
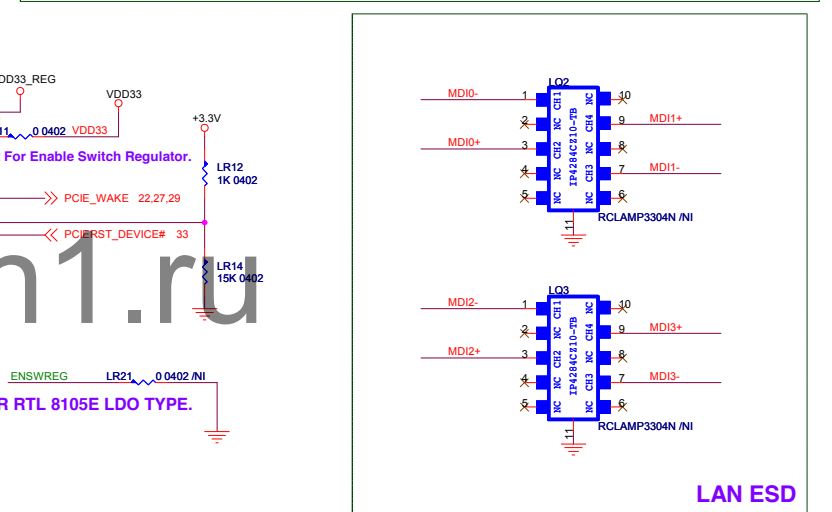
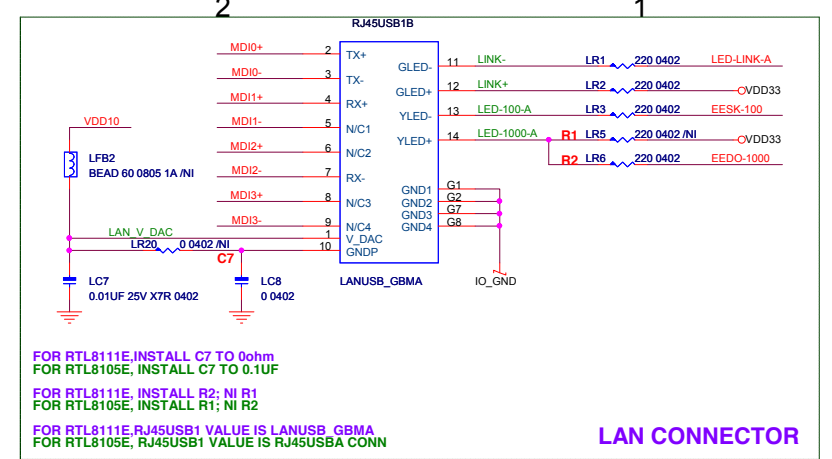
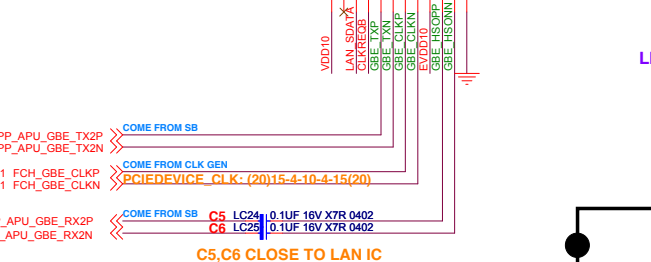
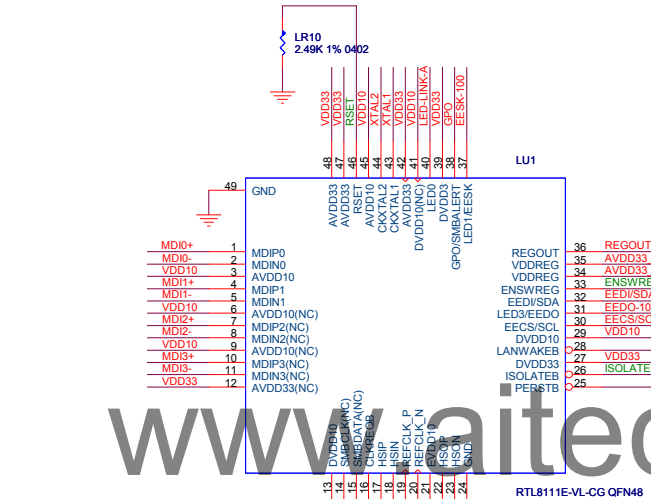
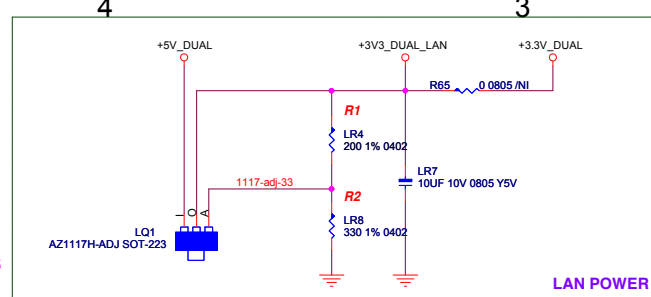
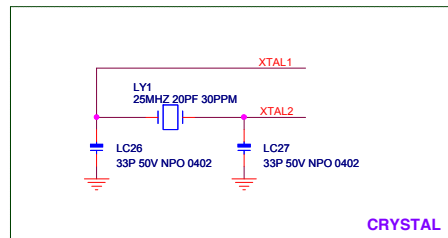
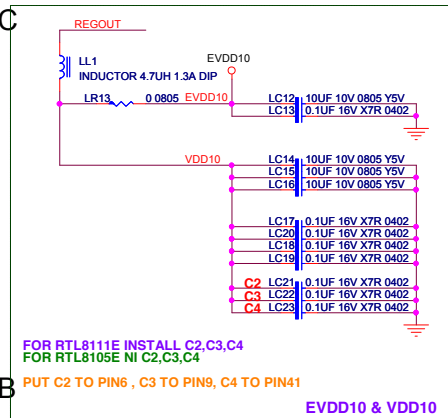
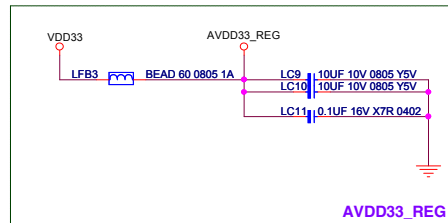
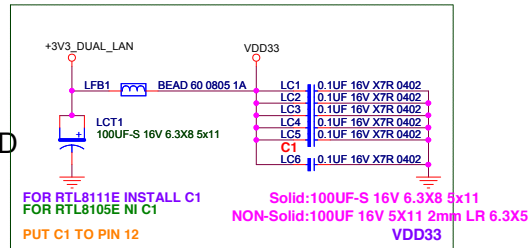
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LAN PART: L+Reference



When using EFuse only without ASF function.

COMPONENT CONTRAST LIST

LAN PARTS	C1	C2	C3	C4	C7	R1	R2	R3	R4	RJ45 CONN
RTL8111E	O	O	O	O	0ohm	X	X	O	O	LANUSB_GBMA
RTL8105E	X	X	X	X	0.1uF	O	O	X	X	RJ45USBA CONN

Access	Blinking	1Gb	Orange
Link	Yellow	100Mb	Green
		10Mb	Off

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